Applied Formal Verification For Digital Circuit Design 1st Edition

ASIC/SoC Functional Design Verification
Equivalence Checking of Digital Circuits
Higher Order Logic Theorem Proving and its Applications
Formal Methods for Industrial Critical Systems
Formal Methods and Their Role in Digital Systems Validation for Airborne Systems
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NASA's Contributions to Aeronautics: Aerodynamics, structures, propulsion, controls
Finding Your Way Through Formal Verification 2nd Edition
Standardized Functional Verification

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ASIC/SoC Functional Design Verification Elsevier
This book constitutes the proceedings of the 26th International Workshop on Formal Methods for Industrial Critical Systems, FMICS 2021, which was held during August 24-26, 2021. The conference was planned to take place in Pairs, France. Due to the COVID-19 pandemic it changed to a virtual event. The 10 full papers and 6 short papers presented in this volume were carefully reviewed and selected from 31 submissions. The papers are organized in topical sections as follows: Verification, Program Safety and Education, (Event-)B Modeling and Validation, Formal Analysis, Tools, Test Generation and Probabilistic Verification.
Equivalence Checking of Digital Circuits McGraw-Hill Companies
Formal methods are a robust approach for problem solving. It is based on logic and algebraic methods where problems can be formulated in a way that can help to find an appropriate solution. This book shows the basic concepts of formal methods and highlights modern modifications and enhancements to provide a more robust and efficient problem solving tool. Applications are

presented from different disciplines such as engineering where the operation of chemical plants is synthesized using formal methods. Computational biology becomes easier and systematic using formal methods. Also, hardware compilation and systems can be managed using formal methods. This book will be helpful for both beginners and experts to get insights and experience on modern formal methods by viewing real applications from different domains.

Higher Order Logic Theorem Proving and its Applications McGraw Hill Professional

Formal Verification: An Essential Toolkit for Modern VLSI Design, Second Edition presents practical approaches for design and validation, with hands-on advice to help working engineers integrate these techniques into their work. Formal Verification (FV) enables a designer to directly analyze and mathematically explore the quality or other aspects of a Register Transfer Level (RTL) design without using simulations. This can reduce time spent validating designs and more quickly reach a final design for manufacturing. Building on a basic knowledge of SystemVerilog, this book demystifies FV and presents the practical applications that are bringing it into mainstream design and validation processes. Every chapter in the second edition has been updated to reflect evolving FV practices and advanced techniques. In addition, a new chapter, Formal Signoff on Real Projects, provides guidelines for implementing signoff quality FV, completely replacing some simulation tasks with significantly more productive FV methods. After reading this book, readers will be prepared to introduce FV in their organization to effectively deploy FV techniques that increase design and validation productivity. Covers formal verification algorithms that help users gain full coverage without exhaustive simulation Helps readers understand formal verification tools and how they differ from simulation tools Shows how to create instant testbenches to gain insights into how models work and to find initial bugs Presents insights from Intel insiders who share their hard-won knowledge and solutions to complex design problems

Formal Methods for Industrial Critical Systems Elsevier

Two-volume collection of case studies on aspects of NACA-NASA research by noted engineers, airmen, historians, museum curators, journalists, and independent scholars. Explores various aspects of how NACA-NASA research took aeronautics from the subsonic to the hypersonic era.-publisher description.

Formal Methods and Their Role in Digital Systems Validation for Airborne Systems Springer Science & Business Media

This report is based on one prepared as a chapter for the FAA Digital Systems Validation Handbook (a guide to assist FAA certification specialists with advanced technology issues). Its purpose is to explain the use of formal methods in the specification and verification of software and hardware requirements, designs, and implementations; to identify the benefits, weaknesses, and difficulties in applying these methods to digital systems used in critical applications; and to suggest factors for consideration when formal methods are offered in support of certification. The presentation concentrates on the rationale for formal methods and on their contribution to assurance for critical applications within a context such as that provided by DO-178B (the guidelines for software used on board civil aircraft); it is intended as an introduction for those to whom

these topics are new. Rushby, John Unspecified Center...
Formal Methods and Their Role in Digital Systems Validation for Airborne Systems Springer Science & Business Media
This book is a solid foundation of the most important formalisms used for specification and verification of reactive systems. In particular, the text presents all important results on m-calculus, w-automata, and temporal logics, shows the relationships between these formalisms and describes state-of-the-art verification procedures for them. It also discusses advantages and disadvantages of these formalisms, and shows up their strengths and weaknesses. Most results are given with detailed proofs, so that the presentation is almost self-contained. Includes all definitions without relying on other material Proves all theorems in detail Presents detailed algorithms in pseudo-code for verification as well as translations to other formalisms
Applied Formal Verification : For Digital Circuit Design Createspace Independent Publishing Platform
There is much excitement in the design and verification community about assertion-based design. The question is, who should study assertion-based design? The emphatic answer is, both design and verification engineers. What may be unintuitive to many design engineers is that adding assertions to RTL code will actually reduce design time, while better documenting design intent. Every design engineer should read this book! Design engineers that add assertions to their design will not only reduce the time needed to complete a design, they will also reduce the number of interruptions from verification engineers to answer questions about design intent and to address verification suite mistakes. With design assertions in place, the majority of the interruptions from verification engineers will be related to actual design problems and the error feedback provided will be more useful to help identify design flaws. A design engineer who does not add assertions to the RTL code will spend more time with verification engineers explaining the design functionality and intended interface requirements, knowledge that is needed by the verification engineer to complete the job of testing the design.
Verification, Validation and Testing in Software Engineering Springer Nature
This volume contains the contributions presented at the International Workshop on Current Trends in Applied Formal Methods organized October 7-9, 1998, in Boppard, Germany. The main objective of the workshop was to draw a map of the key issues facing the practical application of formal methods in industry. This appears to be particularly timely with safety and security issues becoming a real obstacle to industrial software and hardware development. As a consequence, almost all major companies have now set up departments or groups to work with formal methods and many European countries face a severe labour shortage in this new field. Tony Hoare's prediction of the art of software (and hardware) development becoming a proper engineering science with its own body of tools and techniques is now becoming a reality. So the focus of this application oriented workshop was not so much on spe cial academic topics but rather on the many practical aspects of this emerging new technology: verification and validation, and tool support and integration into the software life-cycle. By evaluating the state of the art with respect to industrial applications a discussion emerged among

scientists, practising engi neers, and members of regulatory and funding agencies about future needs and developments. This discussion lead to roadmaps with respect to the future of this field, to tool support, and potential application areas and promising market segments. The contributions of the participants from industry as well as from the respective national security bureaus were particularly valuable and highly appreciated.

Assertion-Based Design Springer Science & Business Media

Formal verification is a powerful new digital design method In this cutting-edge tutorial, two of the field's best known authors team up to show designers how to efficiently apply Formal Verification, along with hardware description languages like Verilog and VHDL, to more efficiently solve real-world design problems.

Formal Hardware Verification Springer Nature

Integrated circuit capacity follows Moore's law, and chips are commonly produced at the time of this writing with over 70 million gates per device. Ensuring correct functional behavior of such large designs before fabrication poses an extremely challenging problem. Formal verification validates the correctness of the implementation of a design with respect to its specification through mathematical proof techniques. Formal techniques have been emerging as commercialized EDA tools in the past decade. Simulation remains a predominantly used tool to validate a design in industry. After more than 50 years of development, simulation methods have reached a degree of maturity, however, new advances continue to be developed in the area. A simulation approach for functional verification can theoretically validate all possible behaviors of a design but requires excessive computational resources. Rapidly evolving markets demand short design cycles while the increasing complexity of a design causes simulation approaches to provide less and less coverage. Formal verification is an attractive alternative since 100% coverage can be achieved; however, large designs impose unrealistic computational requirements. Combining formal verification and simulation into a single integrated circuit validation framework is an attractive alternative. This book focuses on an Integrated Design Validation (IDV) system that provides a framework for design validation and takes advantage of current technology in the areas of simulation and formal verification resulting in a practical validation engine with reasonable runtime. After surveying the basic principles of formal verification and simulation, this book describes the IDV approach to integrated circuit functional validation. Table of Contents: Introduction / Formal Methods Background / Simulation Approaches / Integrated Design Validation System / Conclusion and Summary

Principles of Verifiable RTL Design John Wiley & Sons

This book provides readers with a comprehensive introduction to the formal verification of hardware and software. World-leading experts from the domain of formal proof techniques show the latest developments starting from electronic system level (ESL) descriptions down to the register transfer level (RTL). The authors demonstrate at different abstraction layers how formal methods can help to ensure functional correctness. Coverage includes the latest academic research results, as well as descriptions of industrial tools and case studies.

Correct Hardware Design and Verification Methods Independently Published

From the world's most renowned security technologist, Bruce Schneier, this 20th Anniversary Edition is the most definitive reference on cryptography ever published and is the seminal work on cryptography. Cryptographic techniques have applications far beyond the obvious uses of encoding and decoding information. For developers who need to know about capabilities, such as digital signatures, that depend on cryptographic techniques, there's no better overview than Applied Cryptography, the definitive book on the subject. Bruce Schneier covers general classes of cryptographic protocols and then specific techniques, detailing the inner workings of real-world cryptographic algorithms including the Data Encryption Standard and RSA public-key cryptosystems. The book includes source-code listings and extensive advice on the practical aspects of cryptography implementation, such as the importance of generating truly random numbers and of keeping keys secure. ". . .the best introduction to cryptography I've ever seen. . . .The book the National Security Agency wanted never to be published. . . ." -Wired Magazine ". . .monumental . . . fascinating . . . comprehensive . . . the definitive work on cryptography for computer programmers . . ." -Dr. Dobb's Journal ". . .easily ranks as one of the most authoritative in its field." -PC Magazine The book details how programmers and electronic communications professionals can use cryptography-the technique of enciphering and deciphering messages-to maintain the privacy of computer data. It describes dozens of cryptography algorithms, gives practical advice on how to implement them into cryptographic software, and shows how they can be used to solve security problems. The book shows programmers who design computer applications, networks, and storage systems how they can build security into their software and systems. With a new Introduction by the author, this premium edition will be a keepsake for all those committed to computer and cyber security.

Verification of Reactive Systems Springer Science & Business Media

Formal verification is a powerful new digital design method. In this cutting-edge tutorial, two of the field's best known authors team up to show designers how to efficiently apply Formal Verification, along with hardware description languages like Verilog and VHDL, to more efficiently solve real-world design problems. Contents: Simulation-Based Verification * Introduction to Formal Techniques * Contrasting Simulation vs. Formal Techniques * Developing a Formal Test Plan * Writing High-Level Requirements * Proving High-Level Requirements * System Level Simulation * Design Example * Formal Test Plan * Final System Simulation

Symbolic Simulation Methods for Industrial Formal Verification Springer Science & Business Media

Advanced Formal Verification shows the latest developments in the verification domain from the perspectives of the user and the developer. World leading experts describe the underlying methods of today's verification tools and describe various scenarios from industrial practice. In the first part of the book the core techniques of today's formal verification tools, such as SAT and BDDs are addressed. In addition, multipliers, which are known to be difficult, are studied. The second part gives insight in professional tools and the underlying methodology, such as property checking and assertion based verification. Finally,

analog components have to be considered to cope with complete system on chip designs.

Co-verification of Hardware and Software for ARM SoC Design Springer Science & Business Media

At present the literature gives students and researchers of the very general books on the formal technics. The purpose of this book is to present in a single book, a return of experience on the used of the “formal technics” (such proof and model-checking) on industrial examples for the transportation domain. This book is based on the experience of people which are completely involved in the realization and the evaluation of safety critical system software based. The implication of the industrialists allows to raise the problems of confidentiality which could appear and so allow to supply new useful information (photos, plan of architecture, real example).

Formal Verification of Control System Software Springer

As design complexity in chips and devices continues to rise, so, too, does the demand for functional verification. Principles of Functional Verification is a hands-on, practical text that will help train professionals in the field of engineering on the methodology and approaches to verification. In practice, the architectural intent of a device is necessarily abstract. The implementation process, however, must define the detailed mechanisms to achieve the architectural goals. Based on a decade of experience, Principles of Functional Verification intends to pinpoint the issues, provide strategies to solve the issues, and present practical applications for narrowing the gap between architectural intent and implementation. The book is divided into three parts, each building upon the chapters within the previous part. Part One addresses why functional verification is necessary, its definition and goals. In Part Two, the heart of the methodology and approaches to solving verification issues are examined. Each chapter in this part ends with exercises to apply what was discussed in the chapter. Part Three looks at practical applications, discussing project planning, resource requirements, and costs. Each chapter throughout all three parts will open with Key Objectives, focal points the reader can expect to review in the chapter. * Takes a "holistic" approach to verification issues * Approach is not restricted to one language * Discussed the verification process, not just how to use the verification language

Applied Assertion-Based Verification Springer Science & Business Media

This book grew out of a NATO Advanced Study Institute summer school that was held in Antalya, TUrkey from 26 May to 6 June 1997. The purpose of the summer school was to expose recent advances in the formal verification of systems composed of both logical and continuous time components. The course was structured in two parts. The first part covered theorem-proving, system automaton models, logics, tools, and complexity of verification. The second part covered modeling and verification of hybrid systems, i. e. , systems composed of a discrete event part and a continuous time part that interact with each other in novel ways. Along with advances in microelectronics, methods to design and build logical systems have grown progressively complex. One way to tackle the problem of ensuring the error-free operation of digital or hybrid systems is through the use of formal techniques. The exercise of comparing the formal specification of a logical system namely, what it is supposed to

do to its formal operational description-what it actually does!-in an automated or semi-automated manner is called verification. Verification can be performed in an after-the-fact manner, meaning that after a system is already designed, its specification and operational description are regenerated or modified, if necessary, to match the verification tool at hand and the consistency check is carried out.

Industrial Use of Formal Methods Createspace Independent Publishing Platform

The Integrated Circuit (IC) industry has gone without a standardized verification approach for decades. This book defines a uniform, standardizable methodology for verifying the logical behavior of an integrated circuit, whether an I/O controller, a microprocessor, or a complete digital system. This book will help Engineers and managers responsible for IC development to bring a single, standards-based methodology to their R & D efforts, cutting costs and improving results.

Principles of Functional Verification Elsevier

Hardware veri?cation is the process of checking whether a design conforms to its speci?cations of functionality and timing. In today’s design processes it becomes more and more important. Very large scale integrated (VLSI) circuits and the resulting digital systems have conquered a place in almost all areas of our life, even in security sensitive applications. Complex digital systems control airplanes, have been used in banks and on intensive-care units. Hence, the demand for error-free designs is more important than ever. In addition, economic reasons underline this demand as well. The design and production process of present day VLSI-circuits is highly time- and cost-intensive. Mo- over, it is nearly impossible to repair integrated circuits. Thus, it is desirable to detect design errors early in the design process and not just after producing the prototype chip. All these facts are re?ected by developing and prod- tion statistics of present day companies. For example, In?neon Technologies [118] assumed that about 60% to 80% of the overall design time was spent for veri?cation in 2000. Other sources cite the 3-to-1 head count ratio between veri?cation engineers and logic designers. This shows that verifying logical correctness of the design of hardware systems is a major gate to the problem of time-to-market (cf. [113]). With the chip complexity constantly increasing, the dif?culty as well as the - portance of functional veri?cation of new product designs has been increased. It is not only more important to get error-free designs.

Advanced Formal Verification Now Publishers Inc

CHARME’99 is the tenth in a series of working conferences devoted to the dev- opment and use of leading-edge formal techniques and tools for the design and veri?cation of hardware and systems. Previous conferences have been held in Darmstadt (1984), Edinburgh (1985), Grenoble (1986), Glasgow (1988), Leuven (1989), Torino (1991), Arles (1993), Frankfurt (1995) and Montreal (1997). This workshop and conference series has been organized in cooperation with IFIP WG 10. 5. It is now the biannual counterpart of FMCAD, which takes place every even-numbered year in the USA. The 1999 event took place in Bad Her- nalb, a resort village located in the Black Forest close to the city of Karlsruhe. The validation of functional and timing behavior is a major bottleneck in current VLSI design systems. A predominantly academic area of study until a few years ago,

formal design and veri?cation techniques are now migrating into industrial use. The aim of CHARME'99 is to bring together researchers and users from academia and industry working in this active area of research. Two invited talks illustrate major current trends: the presentation by G´erard Berry (Ecole des Mines de Paris, Sophia-Antipolis, France) is concerned with the use of synchronous languages in circuit design, and the talk given by Peter Jansen (BMW, Munich, Germany) demonstrates an application of formal methods in an industrial environment. The program also includes 20 regular presentations and 12 short presentations/poster exhibitions that have been selected from the 48 submitted papers.