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Journal of Microelectronics and Electronic Packaging
Chiplet Design and Heterogeneous Integration Packaging
Semiconductor Advanced Packaging
Wafer-Level Chip-Scale Packaging
3D IC and RF SiPs: Advanced Stacking and Planar Solutions for 5G Mobility
Lead-free Electronics
Proceedings 1999 International Symposium on Microelectronics
Foldable Flex and Thinned Silicon Multichip Packaging Technology
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2000 International Symposium on Microelectronics
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Structural Dynamics of Electronic and Photonic Systems
Flip Chip, Hybrid Bonding, Fan-In, and Fan-Out Technology
Multiprocessor Systems-on-Chips
Chip On Board
2018 7th Electronic System-Integration Technology Conference (ESTC)

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Journal of Microelectronics and Electronic Packaging Springer
Foldable Flex and Thinned Silicon Multichip Packaging Technology presents newly emerging methods used to make stacked chip packages in the so-called 2-1/2 D technology (3-D in physical format, but interconnected only through the circuits on folded flex). It is also being used in single chip packages where the thinness of the chips and the flex substrate made packages significantly thinner than through any other means.
Chiplet Design and Heterogeneous Integration Packaging Elsevier
This book presents a systematic approach in performing reliability assessment of solder joints using Finite Element (FE) simulation. Essential requirements for FE modelling of an electronic package or a single reflowed solder joint subjected to reliability test conditions are elaborated. These cover assumptions considered for a simplified physical model, FE model geometry development, constitutive models for solder joints and aspects of FE model validation. Fundamentals of the mechanics of solder material are adequately reviewed in relation to FE formulations. Concept of damage is introduced along with deliberation of cohesive zone model and continuum damage model for simulation of solder/IMC interface and bulk solder joint failure, respectively. Applications of the deliberated methodology to selected problems in assessing reliability of solder joints are demonstrated. These industry-defined research-based problems include solder reflow cooling, temperature cycling and mechanical fatigue of a BGA package, JEDEC board-level drop test and mechanisms of solder joint fatigue. Emphasis is placed on accurate quantitative assessment of solder joint reliability through basic understanding of the mechanics of materials as interpreted from results of FE simulations. The FE simulation methodology is readily applicable to numerous other problems in mechanics of materials and structures.
Semiconductor Advanced Packaging John Wiley & Sons
Algorithms for VLSI Physical Design Automation is a core reference text for graduate students and CAD professionals. It provides a comprehensive treatment of the principles and algorithms of VLSI physical design. Algorithms for VLSI Physical Design Automation presents the concepts and algorithms in an intuitive manner. Each chapter contains 3-4 algorithms that are discussed in detail. Additional algorithms are presented in a somewhat shorter format. References to advanced algorithms are presented at the end of each chapter. Algorithms for VLSI Physical Design Automation covers all aspects of physical design. The first three chapters provide the background material while the subsequent chapters focus on each phase of the physical design cycle. In addition, newer topics like physical design automation of FPGAs and MCMs have been included. The author provides an extensive bibliography which is useful for finding

advanced material on a topic. Algorithms for VLSI Physical Design Automation is an invaluable reference for professionals in layout, design automation and physical design.

Wafer-Level Chip-Scale Packaging
Springer Nature
Microelectronic packaging has been recognized as an important "enabler" for the solid state revolution in electronics which we have witnessed in the last third of the twentieth century. Packaging has provided the necessary external wiring and interconnection capability for transistors and integrated circuits while they have gone through their own spectacular revolution from discrete device to gigascale integration. At IBM we are proud to have created the initial, simple concept of flip chip with solder bump connections at a time when a better way was needed to boost the reliability and improve the manufacturability of semiconductors. The basic design which was chosen for SLT (Solid Logic Technology) in the 1960s was easily extended to integrated circuits in the '70s and VLSI in the '80s and '90s. Three I/O bumps have grown to 3000 with even more anticipated for the future. The package families have evolved from thick-film (SLT) to thin-film (metallized ceramic) to co-fired multi-layer ceramic. A later family or ceramics with matching expansivity to sili con and copper internal wiring was developed as a predecessor of the chip interconnection revolution in copper, multilevel, submicron wiring. Powerful server packages have been de veloped in which the combined chip and package copper wiring exceeds a kilometer. All of this was achieved with the constant objective of minimizing circuit delays through short, efficient interconnects.
3D IC and RF SiPs: Advanced Stacking and Planar Solutions for 5G Mobility
Springer Science & Business Media
Fracture, Fatigue, Failure and Damage Evolution, Volume 8 of the Proceedings of the 2016 SEM Annual Conference & Exposition on Experimental and Applied Mechanics, the eighth volume of ten from the Conference, brings together contributions to this important area of research and engineering. The collection presents early findings and case studies on a wide range of areas, including: In-situ Techniques for Fracture & Fatigue General Topics in Fracture & Fatigue Fracture & Fatigue of Composites Damage, Fracture, Fatigue & Durability Interfacial Effects in Fracture & Fatigue Damage Detection in Fracture & Fatigue
Lead-free Electronics CRC Press
This book examines electronics reliability and measurement technology. It identifies advances in measurement science and technology for nondestructive evaluation, and it details common measurement trouble spots.
Proceedings 1999 International Symposium on Microelectronics Springer Science & Business Media
Lead-free Electronics provides guidance on the design and use of lead-free electronics as well as technical and legislative perspectives. All the complex challenges confronting the elec-tronics industry are skillfully addressed: * Complying with state legislation * Implementing the transition to lead-free electronics, including anticipating associated costs and potential supply chain issues * Understanding intellectual property issues in lead-free alloys and their applications, including licensing and infringement * Implementing cost effective manufacturing and testing * Reducing risks due to tin whiskers * Finding lead-free solutions in harsh environments such as in the automotive

and telecommunications industries * Understanding the capabilities and limitations of conductive adhesives in lead-free interconnects * Devising solutions for lead-free, flip-chip interconnects in high-performance integrated circuit products Each chapter is written by leading experts in the field and carefully edited to ensure a consistent approach. Readers will find all the latest information, including the most recent data on cyclic thermomechanical deformation properties of lead-free SnAgCu alloys and a comparison of the properties of standard Sn-Pb versus lead-free alloys, using the energy partitioning approach. With legislative and market pressure to eliminate the use of lead in electronics manufacturing, this timely publication is essential reading for all engineers and professionals in the electronics industry.

Foldable Flex and Thinned Silicon Multichip Packaging Technology
Springer Science & Business
Examines the advantages of Embedded and FO-WLP technologies, potential application spaces, package structures available in the industry, process flows, and material challenges Embedded and fan-out wafer level packaging (FO-WLP) technologies have been developed across the industry over the past 15 years and have been in high volume manufacturing for nearly a decade. This book covers the advances that have been made in this new packaging technology and discusses the many benefits it provides to the electronic packaging industry and supply chain. It provides a compact overview of the major types of technologies offered in this field, on what is available, how it is processed, what is driving its development, and the pros and cons. Filled with contributions from some of the field's leading experts,Advances in Embedded and Fan-Out Wafer Level Packaging Technologies begins with a look at the history of the technology. It then goes on to examine the biggest technology and marketing trends. Other sections are dedicated to chip-first FO-WLP, chip-last FO-WLP, embedded die packaging, materials challenges, equipment challenges, and resulting technology fusions. Discusses specific company standards and their development results Content relates to practice as well as to contemporary and future challenges in electronics system integration and packaging Advances in Embedded and Fan-Out Wafer Level Packaging Technologies will appeal to microelectronic packaging engineers, managers, and decision makers working in OEMs, IDMs, IFMs, OSATs, silicon foundries, materials suppliers, equipment suppliers, and CAD tool suppliers. It is also an excellent book for professors and graduate students working in microelectronic packaging research.

Guidebook for Managing Silicon Chip Reliability Springer
Advanced Flip Chip Packaging presents past, present and future advances and trends in areas such as substrate technology, material development, and assembly processes. Flip chip packaging is now in widespread use in computing, communications, consumer and automotive electronics, and the demand for flip chip technology is continuing to grow in order to meet the need for products that offer better performance, are smaller, and are environmentally sustainable.

Chip Scale Package (CSP) Springer Science & Business Media
Modeling, Analysis, Design and Testing for Electronics Packaging Beyond Moore

provides an overview of electrical, thermal and thermomechanical modeling, analysis, design and testing for 2.5D/3D. The book addresses important topics, including electrically and thermally induced issues, such as EMI and thermal issues, which are crucial to package signal and thermal integrity. It also covers modeling methods to address thermomechanical stress related to the package structural integrity. In addition, practical design and test techniques for packages and systems are included. Includes advanced modeling and analysis methods and techniques for state-of-the art electronics packaging Features experimental characterization and qualifications for the analysis and verification of electronic packaging design Provides multiphysics modeling and analysis techniques of electronic packaging

Lead Free Solder Springer

The book focuses on the design, materials, process, fabrication, and reliability of advanced semiconductor packaging components and systems. Both principles and engineering practice have been addressed, with more weight placed on engineering practice. This is achieved by providing in-depth study on a number of major topics such as system-in-package, fan-in wafer/panel-level chip-scale packages, fan-out wafer/panel-level packaging, 2D, 2.1D, 2.3D, 2.5D, and 3D IC integration, chiplets packaging, chip-to-wafer bonding, wafer-to-wafer bonding, hybrid bonding, and dielectric materials for high speed and frequency. The book can benefit researchers, engineers, and graduate students in fields of electrical engineering, mechanical engineering, materials sciences, and industry engineering, etc.

Interconnect Reliability in Advanced Memory Device Packaging Springer Nature

This text comprises the proceedings of the 1999 International Symposium on Microelectronics.

Advances in Embedded and Fan-Out Wafer Level Packaging Technologies McGraw Hill Professional

This text constitutes proceedings from the International Symposium on Microelectronics that took place in Boston, Massachusetts in September, 2000.

Fracture, Fatigue, Failure and Damage Evolution, Volume 8 Springer Nature

This book offers a comprehensive reference guide for graduate students and professionals in both academia and industry, covering the fundamentals, architecture, processing details, and applications of 3D microelectronic packaging. It provides readers an in-depth understanding of the latest research and development findings regarding this key industry trend, including TSV, die processing, micro-bumps for LMI and MMI, direct bonding and advanced materials, as well as quality, reliability, fault isolation, and failure analysis for 3D microelectronic packages. Images, tables, and didactic schematics are used to illustrate and elaborate on the concepts discussed. Readers will gain a general grasp of 3D packaging, quality and reliability concerns, and common causes of failure, and will be introduced to developing areas and remaining gaps in 3D packaging that can help inspire future research and development.

Algorithms for VLSI Physical Design Automation Woodhead Publishing

An interdisciplinary guide to enabling technologies for 3D ICs and 5G mobility, covering packaging, design to product

life and reliability assessments Features an interdisciplinary approach to the enabling technologies and hardware for 3D ICs and 5G mobility Presents statistical treatments and examples with tools that are easily accessible, such as Microsoft’s Excel and Minitab Fundamental design topics such as electromagnetic design for logic and RF/passives centric circuits are explained in detail Provides chapter-wise review questions and powerpoint slides as teaching tools
Heterogeneous Integrations Springer Science & Business Media
Featuring the latest design techniques, plus details on more than 40 different types of CSP, hands engineers and designers the complete, professional set of working tools to: solve technical and design issues; find the most efficient, cost-effective CSP solutions for deployments; answer questions on interfacing, speed, robustness, and more; compare properties of wirebonds, flip chips, rigid and flex substrates, wafer-level redistribution, and other CSP products; get the latest information on new offerings from Fujitsu, GE, Hitachi, IBM, and other major companies; and learn about CSP products under development.
MEMS, NANO and Smart Systems John Wiley & Sons
The proposed book will offer comprehensive and versatile methodologies and recommendations on how to determine dynamic characteristics of typical micro- and opto-electronic structural elements (printed circuit boards, solder joints, heavy devices, etc.) and how to design a viable and reliable structure that would be able to withstand high-level dynamic loading. Particular attention will be given to portable devices and systems designed for operation in harsh environments (such as automotive, aerospace, military, etc.) In-depth discussion from a mechanical engineer's viewpoint will be conducted to the key components’ level as well as the whole device level. Both theoretical (analytical and computer-aided) and experimental methods of analysis will be addressed. The authors will identify how the failure control parameters (e.g. displacement, strain and stress) of the vulnerable components may be affected by the external vibration or shock loading, as well as by the internal parameters of the infrastructure of the device. Guidelines for material selection, effective protection and test methods will be developed for engineering practice.
Modeling, Analysis, Design, and Tests for Electronics Packaging beyond Moore John Wiley & Sons
Analog and Power Wafer Level Chip Scale Packaging presents a state-of-art and in-depth overview in analog and power WLCSP design, material characterization, reliability and modeling. Recent advances in analog and power electronic WLCSP packaging are presented based on the development of analog technology and power device integration. The book covers in detail how advances in semiconductor content, analog and power advanced WLCSP design, assembly, materials and reliability have co-enabled significant advances in fan-in and fan-out with redistributed layer (RDL) of analog and power device capability during recent years. Since the analog and power electronic wafer level packaging is different from regular digital and memory IC package, this book will systematically introduce the typical analog and power electronic wafer level packaging design, assembly

process, materials, reliability and failure analysis, and material selection. Along with new analog and power WLCSP development, the role of modeling is a key to assure successful package design. An overview of the analog and power WLCSP modeling and typical thermal, electrical and stress modeling methodologies is also presented in the book.

Dynamic Behavior of Materials, Volume 1 Springer

This book is a one-stop guide to the state of the art of COB technology. For professionals active in COB and MCM research and development, those who wish to master COB and MCM problem-solving methods, and those who must choose a cost-effective design and high-yield manufacturing process for their interconnect systems, here is a timely summary of progress in al aspects of this fascinating field. It meets the reference needs of design, material, process, equipment, manufacturing, quality, reliability, packaging, and system engineers, and technical managers working in electronic packaging and interconnection.

Harsh Environment Electronics

Springer Nature

Dynamic Behavior of Materials, Volume 1: Proceedings of the 2012 Annual Conference on Experimental and Applied Mechanics represents one of seven volumes of technical papers presented at the Society for Experimental Mechanics SEM 12th International Congress & Exposition on Experimental and Applied Mechanics, held at Costa Mesa, California, June 11-14, 2012. The full set of proceedings also includes volumes on Challenges in Mechanics of Time -Dependent Materials and Processes in Conventional and Multifunctional Materials, Imaging Methods for Novel Materials and Challenging Applications, Experimental and Applied Mechanics, 2nd International Symposium on the Mechanics of Biological Systems and Materials 13th International Symposium on MEMS and Nanotechnology and, Composite Materials and the 1st International Symposium on Joining Technologies for Composites.

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