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The UVM 1.1 Class Reference represents the foundation used to create the UVM 1.1 User's Guide.

This guide is a way to apply the UVM 1.1 Class Reference, but is not the only way. Accellera

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Introduction. UVM is a methodology for the functional verification of digital hardware, primarily using simulation. The hardware or system to be verified would typically be described using Verilog, SystemVerilog, VHDL or SystemC at any appropriate abstraction level. This could be behavioral, register transfer level, or gate level.

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