Design Of A 60ghz Low Noise Amplier In Sige Technology

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Ultra-Wideband and 60 GHz Communications for Biomedical Applications Springer Science & Business Media
The book is a dissertation entitled "Design of Fully Integrated 60 GHz OFDM Transmitter in SiGe BiCMOS Technology." It presents transmitter design for wireless communication in the ISM band at 60 GHz for speeds of several Gbit/s. It is focused on design of transmitter components, which are critical for the performance of the whole analog front-end. Phase-locked loop phase noise optimization is presented. A new optimized recipe for calculating phase-locked loop parameters of a forth order PLL is presented, resulting in the spurious sideband reduction by up to 10 dB. The design of integrated image-rejection filters with low quality factor of the integrated resonators is presented. The challenges related to the design of mm-wave power amplifiers with high P1dB are analyzed and the procedure of the PA design is presented. The fully integrated transmitter was used for data transmission with data rate of 3.6 Gbit/s (with coding 4.8 Gbit/s) over 15 meters. This is the best result in the class of 60 GHz analog front-ends without beamforming.
Design and Integration of 60-GHz Grid Array Antenna in Chip Package Springer Nature
This book describes the design of a receiver front-end circuit for operation in the 60GHz range in 90nm CMOS. Physical layout of the test circuit and post-layout simulations for the implementation of a test chip including the QVCO and the first stage divider are also presented. The content of this book is particularly of interest to those working on mm-wave frequency generation and signal reception.
UWB Communication Systems: Conventional and 60 GHz Springer Science & Business Media
This book addresses 60 GHz technology for Gbps WLAN and WPAN from theory to practice, covering key aspects for successful deployment. In this book, the authors focus specifically on 60 GHz wireless technology which has emerged as the most promising candidate for multi-gigabit wireless indoor communication systems. 60 GHz technology offers various advantages over current or existing communications systems (e.g. huge unlicensed bandwidth worldwide, high transmit power, high frequency reuse and small form factor), which enables many disruptive applications that are otherwise difficult if not impossible to be realized at lower frequencies. The book addresses all aspects of the state-of-the-art in 60 GHz technology for high data rate wireless applications. Key Features: Comprehensive coverage from theory to practice: provides readers with a thorough technical guide of 60 GHz technology development Brings together the entire area of 60GHz technology for Gigabits per second (Gbps) WLAN and WPAN applications. Discusses practical system designs covering wide aspects such as antenna propagation, beamforming, circuit design, digital communication, signal processing, system architectures, etc. Provides up-to-date standardization activities, regulatory issues, technology development as well as future trends Includes examples and case studies for practical scenarios Contains theoretical, simulation and experimental results to demonstrate and compare the performance of various schemes (or systems) This book serves as an excellent reference for system engineers, system architects, IC designers, standard engineers, researchers, and vendor and manufacturer consumers. Technical consultants, software and application developers will also find this book of interest.
Emerging Technologies and Circuits Springer
This book investigates the design of devices, systems, and circuits for medical applications using the two recently established frequency bands: ultra-wideband (3.1-10.6 GHz) and 60 GHz ISM band. These two bands provide the largest bandwidths available for communication technologies and present many attractive opportunities for medical applications. The applications of these bands in healthcare are wireless body area network (WBAN), medical imaging, biomedical sensing, wearable and implantable devices, fast medical device connectivity, video data transmission, and vital signs monitoring. The recent technological advances and developments proposed or used in medicine based on these two bands are covered. The book introduces possible solutions and design techniques to efficiently implement these systems in medical environment. All individual chapters are written by leading experts in their fields. Contributions by authors are on various applications of ultra-wideband and the 60 GHz ISM band including circuit implementation, UWB and 60 GHz signal transmission around and in-body, antenna design solution, hardware implementation of body sensors, UWB transceiver design, 60 GHz transceiver design, UWB radar for contactless respiratory monitoring, and ultra-wideband based medical Imaging. The book will be a key resource for medical professionals, bio-medical engineers, and graduate and senior undergraduate students in computer, electrical, electronic and biomedical engineering disciplines.
Analog Circuit Design Springer Science & Business Media
Abstract: Emerging broadband applications are pushing for the need to build high data rate wireless transceivers at 60GHz for high volume low cost mobile devices. Central to the success of implementing such transceivers is the robust design of 60GHz CMOS RF front ends, especially the low noise amplifiers (LNAs). In the future, CMOS technology is expected to enable low-cost mm-wave applications such as high data-rate communication links, passive and active imaging and sensor systems, and instrumentation and measurements equipment. Building highly integrated inexpensive mm-wave CMOS devices requires high quality factor lumped and distributed passives with accurate and scalable transistor and passives models. My research work focuses on demonstrating a methodology for generating a scalable compact model for on-chip transmission lines and interconnects on lossy silicon substrate. The model is demonstrated over 20-60 GHz frequency band using two types of transmission lines built in TSMC's 0.18 um CMOS technology. Several CPWs and Microstrip lines are designed with different lengths to verify the accuracy and scalability of the extracted model. The compact model shows an excellent agreement with measured data with maximum deviation in S11 magnitude and phase of 9.2% and 5.6%, respectively, and maximum deviation in S21 magnitude and phase of 10.1% and 6.6%, respectively. Compared to existing model extraction methodologies, the required time for generating the compact model and simulating transmission lines is reduced significantly. The generated models are fully compatible with all commercial circuit simulators. This work presents key design techniques for different CMOS mm-wave LNA topologies. The proposed LNA topologies are, the three-stage cascode RF NMOS configuration and four-stage Common Gate followed by Common Source configuration. Simulation results for 60GHz LNAs show that the first topology can achieve a peak gain of 16.67 dB with a 3-dB bandwidth of 7 GHz, and a noise figure less than 11.04 dB over the entire bandwidth. The achieved peak gain from the second topology is 9.7 dB with a 3-dB bandwidth of 7 GHz and a noise figure less than 13.06 dB over the entire bandwidth. Simulation results for Sub-THz LNAs show that the first topology can achieve a peak gain of 23.5 dB at 92.1 GHz with a 3-dB bandwidth of 25 GHz, and a noise figure less than 5.5 dB over the entire bandwidth. The achieved peak gain from the second topology is 23.2 dB at 105 GHz with a 3-dB bandwidth of 15 GHz and a noise figure less than 6.1 dB over the entire bandwidth. The LNAs are designed and tested in 90nm RF CMOS. Moreover in today's radio design environment, the front-end analog devices in the transceiver require several silicon spins before they meet the specifications and they have relatively low yields. My work aims to propose a digital self-calibration technique for LNAs' to enhance the yield to at least 90%. The proposed technique is shown to maintain typical specified performance at worst case corners in the presence of random process, supply and temperature variations, and hence allowing for manufacturable 60GHz RF CMOS design for high volume applications without leading to over-design or increasing power

consumption.

60 GHz CMOS Pico-joule/bit OOK Receiver Design for Multi-gigabit Per Second Wireless Communications IGI Global

A transistor-level, design-intensive overview of high speed and high frequency monolithic integrated circuits for wireless and broadband systems from 2 GHz to 200 GHz, this comprehensive text covers high-speed, RF, mm-wave, and optical fibre circuits using nanoscale CMOS, SiGe BiCMOS, and III-V technologies. Step-by-step design methodologies, end-of chapter problems, and practical simulation and design projects are provided, making this an ideal resource for senior undergraduate and graduate courses in circuit design. With an emphasis on device-circuit topology interaction and optimization, it gives circuit designers and students alike an in-depth understanding of device structures and process limitations affecting circuit performance.

Design of 60ghz 65nm CMOS Power Amplifier Cambridge University Press

This book focuses on the development of design techniques and methodologies for 60-GHz and E-band power amplifiers and transmitters at device, circuit and layout levels. The authors show the recent development of millimeter-wave design techniques, especially of power amplifiers and transmitters, and presents novel design concepts, such as “power transistor layout” and “4-way parallel-series power combiner”, that can enhance the output power and efficiency of power amplifiers in a compact silicon area. Five state-of-the-art 60-GHz and E-band designs with measured results are demonstrated to prove the effectiveness of the design concepts and hands-on methodologies presented. This book serves as a valuable reference for circuit designers to develop millimeter-wave building blocks for future 5G applications.

Design of a Low-cost 60 GHz Transceiver Frontend Springer Science & Business Media

Abstract This chapter lays the foundation for the work presented in latter chapters. The potential of 60 GHz frequency bands for high data rate wireless transfer is discussed and promising applications are enlisted. Furthermore, the challenges related to 60 GHz IC design are presented and the chapter concludes with an outline of the book. Keywords Wireless communication 60 GHz Millimeter wave integrated circuit design Phase-locked loop CMOS Communication technology has revolutionized our way of living over the last century. Since Marconi’s transatlantic wireless experiment in 1901, there has been tremendous growth in wireless communication evolving from spark-gap telegraphy to today’s mobile phones equipped with Internet access and multimedia capabilities. The omnipresence of wireless communication can be observed in widespread use of cellular telephony, short-range communication through wireless local area networks and personal area networks, wireless sensors and many others. The frequency spectrum from 1 to 6 GHz accommodates the vast majority of current wireless standards and applications. Coupled with the availability of low cost radio frequency (RF) components and mature integrated circuit (IC) techn- ogies, rapid expansion and implementation of these systems is witnessed. The downside of this expansion is the resulting scarcity of available bandwidth and allowable transmit powers. In addition, stringent limitations on spectrum and energy emissions have been enforced by regulatory bodies to avoid interference between different wireless systems.

Gigabit Wireless at 60 Ghz LAP Lambert Academic Publishing

This book constitutes the proceedings of the 26th International Symposium on VLSI Design and Test, VDAT 2022, which took place in Jammu, India, in July 2022. The 32 regular papers and 16 short papers presented in this volume were carefully reviewed and selected from 220 submissions. They were organized in topical sections as follows: Devices and Technology; Sensors; Analog/Mixed Signal; Digital Design; Emerging Technologies and Memory; System Design.

Design and Implementation of High Gain 60 GHz Antennas for Imaging/Detection Systems Springer Science & Business Media

Telecommunication industry claims for increasing data rate in wireless communication systems. The major demand of high data rate applications concerns a large panel of home multimedia exchanging data especially for the uncompressed HD data transfer. The 7GHz band around 60GHz is free of use and fulfils the short range gigabit communication requirements. CMOS technology is most appropriate since it drives a fast time to market with a low cost for high integration volume. However, the use of CMOS technology is challenging to satisfy loss and performance trade-off under power constraints. This thesis aims at designing power amplifiers operating at 60GHz with 65nm CMOS technology from STMicroelectronics. This approach is progressive because it is necessary to analyze and optimize the performance of passive and active components constituting the power amplifier using electromagnetic and microelectronics software. Finally, power amplifiers have been made. Their performances met specifications originally defined.

High-Frequency Integrated Circuits Springer Science & Business Media

This book includes high-quality research papers presented at the Fourth International Conference on Communication, Computing and Electronics Systems (ICCCES 2022), held at the PPG Institute of Technology, Coimbatore, India, on September 15–16, 2022. The book focuses mainly on the research trends in cloud computing, mobile computing, artificial intelligence and advanced electronics systems. The topics covered are automation, VLSI, embedded systems, optical communication, RF communication, microwave engineering, artificial intelligence, deep learning, pattern recognition, communication networks, Internet of things, cyber-physical systems and healthcare informatics.

Integrated 60GHz RF Beamforming in CMOS CRC Press

Recent technology advances are poised to enable low-cost, low-power communications in the 7 GHz of unlicensed spectrum at 60 GHz millimeter wave (mmW) frequencies. However, mmW systems that meet the Gb/s data rate demands of wireless multimedia applications must overcome severe propagation effects, including high path loss and high diffraction loss. Consequently, nodes in the network will have to use directional antennas. The narrow main beam widths of directional antennas introduce design challenges for Medium Access Control (MAC) protocols but, at the same time, provide opportunities for routing protocols to improve the network capacity through better spatial reuse. The small wavelength of a 60 GHz signal can help to achieve high directional antenna gain, but it also precludes diffraction around humans, furniture, and similarly-sized objects. These obstacles penalize a 60 GHz link budget by 20-30dB. Therefore, when people are in motion, 60 GHz network links go on and off frequently due to human body blockage; this introduces new design challenges for both routing and transport protocols. In this dissertation, we propose solutions at the MAC and network layer to address the above challenges. In particular, we first propose an enhanced directional MAC (EDMAC) to resolve the unfairness and low channel utilization issues of deafness in directional MAC protocols for 60 GHz networks. We then study single path routing and find that shortest path routing often fails to exploit the high spatial reuse properties of directional antennas. We propose two heuristic routing algorithms, namely HOP-FP and FP-HOP, which combine the fattest-path (FP) and minimum-hop (HOP) metrics, with and without the consideration of interference. We then employ multipath routing for 60 GHz networks to fully utilize the high spatial reuse property of directional antennas. We develop an online node-disjoint path discovery process to find multiple node-disjoint paths between the source and the destination without knowledge of the global topology. In addition, we model the characteristics of link outages that are induced by pedestrian blockage. Based on analytic models and MATLAB simulation results, we show that link blockages can be mitigated by multipath routing schemes with blockage timers for broken paths. We use the ns-2 simulator to validate all proposed protocols in this dissertation.

Analysis and Design of 60GHz CMOS Low Noise Amplifier Springer

The world-wide availability of the huge amount of license-free spectral space in the 60 GHz band provides wide room for Gb/s wireless applications. A commercial (read: low-cost) 60-GHz transceiver will, however, provide limited system performance due to the stringent link budget and the substantial RF imperfections. This book comprises research into the characteristics of typical 60-GHz channels, the influence of directional antenna patterns, the evaluation of the wideband transmission quality as well as the development of suitable baseband algorithms in the context of 60-GHz radios. A baseline system design is illustrated by taking into account the particular properties of the channel, antennas and RF front-ends. Both experimental results and theoretical derivations are provided to support each other. This book, therefore, should be a valuable reference for wireless researchers and designers, especially for those who are interested in the design of gigabit 60-GHz radios.

Design and Performance Analysis of Switched Beam Series-fed Patch Antenna Array for 60GHz WPAN Applications Sudwestdeutscher Verlag Fur Hochschulschriften AG

Analog Circuit Design is based on the yearly Advances in Analog Circuit Design workshop. The aim of the workshop is to bring together designers of advanced analogue and RF circuits for the purpose of studying and discussing new possibilities and future developments in this field. Selected topics for AACD 2007 were: (1) Sensors, Actuators and Power Drivers for the Automotive and Industrial Environment; (2) Integrated PA's from Wireline to RF; (3) Very High Frequency Front Ends.

Proceedings of Fourth International Conference on Communication, Computing and Electronics Systems CRC Press

Increased memory capacity and processing power in mobile devices has created a need for radios that can transmit data at multi-Gb/s rates over a short range. However, battery capacity has not kept pace with these advances so power consumption must be kept to a minimum to maintain long battery life. Furthermore, consumer devices require low cost components due to the strong market pressures continuously driving down Average Selling Prices (ASP) leading to diminishing margins. This means a fully integrated solution including RF and baseband components is more attractive than a modular solution. The allocation of 7GHz of unlicensed bandwidth in the 60GHz band and the increasing speed of CMOS technology provides an excellent opportunity for low cost, high data rate, fully integrated radios to fulfill the unique requirements of modern mobile devices. Phased array transceivers using simple modulation schemes should be used due to their high energy efficiency. Phased arrays use spatial power combining to help overcome the high path loss at 60GHz and also provide beam-steering capabilities which can help to overcome fading issues and create a secure means of communication. Significant progress has been been made recently in the design of mm-wave CMOS building blocks and transceivers, including some phased array transceivers. However, very little attention has been paid to systematic optimization and design of the LO generation and distribution subsystem. In this thesis we use the baseband phase shifting architecture as a vehicle for optimizing LO generation and distribution in phased array transceivers. We propose strategies for optimal low power design with a focus on holistic optimization from architectural choices down to block level design resulting in an optimal and scalable LO distribution methodology. Finally, we present sample designs of building blocks such as oscillators and phase locked loops as well as a full LO generation and distribution subsystem for a 4-element baseband phased-array transceiver in a standard digital 65nm CMOS process.

Data Transmission at Millimeter Waves Springer

Component design for a proposed 60 GHz short-range low-power high-data-rate On-Off Keying receiver in a 90 nm CMOS process is presented. The advances in RFCMOS and the commercial need for high data-rate wireless links are discussed as the enabling technology and motivation for research into the development of 60 GHz CMOS radios for wireless personal area networks. System level calculations are presented validating the feasibility of the proposed receiver topology for its target application. The design and simulation results of a 60 GHz low noise amplifier, 60 GHz direct-conversion demodulator (which has generated an invention disclosure), and a baseband amplifier are discussed in detail. Also presented is a discussion of device modeling techniques for millimeter-wave designs. Measured results are presented for the demodulator. Finally, recommendations for future work are presented.

Design of Fully Integrated 60GHz OFDM Transmitter Springer Nature

This project gives a detailed study of the Design and Performance analysis of series fed patch antenna array for 60 GHz system applications. The patch array designed in this project will act as an active element and can be used as the feed antenna of the dielectric flat lens antenna which is highly directive at 60 GHz. CPW (Coplanar Waveguide) is used as the feeding technique of the antenna array because it has lower transmission loss, lower profile especially on high frequency band. The purpose of the array is to perform the beam scanning with the shift in the frequency over the complete range of V-Band i.e. 57 GHz to 64 GHz. The designs are simulated in HFSS which is a high frequency simulator for designing such antennas. Due to the low profile and small weight of these antennas, they are constructed in microstrip technology which allows easy integration with printed circuits. For the fabrication of antennas Laser machine LPKF and photolithographic process are used.

Handbook of Research on Advanced Trends in Microwave and Communication Engineering John Wiley & Sons

This book shows that with the use of metamaterials, one can have coherent THz signal generation, amplification, transmission, and detection for phase-arrayed CMOS transistors with significantly improved performance. Offering detailed coverage from device to system, the book describes the design and application of metamaterials in actual CMOS integrated circuits, includes real circuit examples and chip demonstrations with measurement results, and also evaluates system performance after CMOS-based system-on-chip integration. The book reflects the latest research progress and provides a state-of-the-art reference on CMOS-based metamaterial devices and mm-wave and THz systems.

60-GHz CMOS Phase-Locked Loops Springer

Research in the mm-wave band using CMOS and SiGe technologies has gained momentum over the past few years. Millimeter-wave circuits are expected to enter consumer electronics in the near future. 60GHz circuits have the potential to be used in high definition wireless video transmission and high data-rate point-to-point communication. 77GHz has been explored for automotive radar and is expected to become more ubiquitous in coming years. 90GHz has been investigated for imaging and remote sensing applications. Raw silicon transistor performance has improved dramatically in the past decade, which has spurred much of the research. The potential low cost of silicon ICs, especially CMOS, is great motivation to design mm-wave circuits for volume production. This dissertation is divided into two parts. In the first part, the design of a 60GHz CMOS receiver is presented. Design methodologies for robust operation at 60GHz are introduced at device and circuit levels. Key building blocks of a 60GHz receiver are investigated and several design techniques are proposed to increase the performance of the 60GHz circuits. Second part explores the potential of mm-wave design for imaging applications. Performance requirements and challenges of a 90GHz power amplifier for imaging applications are explored.

Circuit and system level design details of a pulsed power amplifier are provided and methodologies for enhancing the performance of those designs are introduced. In the end, A prototype of this power amplifier and its integrated version in an ultra wideband pulsed transmitter are presented. This thesis is expected to provide a design framework for achieving predictable and desired performance at mm-wave band.

Energy-Efficient 60GHz Phased-Array Design for Multi-Gb/s Communication Systems CRC Press

Recent advance in wireless technologies has enabled rapid growth of mobile devices. Consequently, emerging applications for mobile devices have begun demanding data rates up to multiple Gb/s. Although advanced WiFi systems are approaching such data rates, the narrow bandwidth at ISM band fundamentally limits the achievable data-rate. Therefore, the unlicensed 7GHz of bandwidth at 60GHz band provides an opportunity to efficiently implement these communication systems with a potential to achieve $>$10Gb/s throughput. Besides the wider bandwidth, operating at higher frequency theoretically has higher achievable signal-to-noise ratio in area limited applications. This is because the maximum achievable antenna gain within limited aperture increases with frequency and it can be achieved using phased-array technique. This thesis therefore focuses on the design of 60GHz phased-array transceivers to support energy-efficient high data-rate communication systems. Despite the advantages of 60GHz, mobile applications often require low power consumption as well as low cost implementation, making the design of 60GHz phased-array systems challenging. Taking into account the limited power budget, this research investigates the design choices of the number of elements in phased-array transceivers, and identifies that the overhead power is the bottleneck of energy efficiency. In order to reduce the overhead power in the transmitter, a new architecture using a fast start-up oscillator is proposed, which eliminates the need of explicit modulator and 60GHz LO delivery. Measurements has shown that the transmitter efficiency is boosted by more than 2X. More importantly, the overhead power is significantly reduced down to 2mW, making this architecture a good candidate for large number phased-array. On the other hand, suffering from the similar overhead problem, the receiver unfortunately could not share the same architecture. A different architecture that stacks the mixer on top of LO generation is thus proposed to reduce the power consumption in the receiver. This approach demonstrated a 2X power reduction in receiver overhead, and the resulted optimum number of receiver elements is close to 4. Besides using CMOS technologies, on-chip antenna is also studied in order to further reduce the system cost. Slot-loop antenna is identified as a good candidate because that its intrinsic ground plane eases the integration with the rest of circuitry. Although the simulation shows an efficiency as high as 30%, the planar nature of the on-chip antenna limits its coverage in end-fire directions. Antenna diversity is thus proposed to overcome this limitation by utilizing multiple drive points on the same antenna. Because the antenna is fully integrated on-chip, antenna diversity can be implemented without extra high frequency I/Os, eliminating the loss that would be introduced otherwise. Using the proposed transceiver architectures, a 4-element phased-array with on-chip antennas was fabricated on TSMC's 65nm CMOS technology as a test vehicle. Consuming 50mW in the transmitter and 65mW in the receiver, this 10.4Gb/s phased-array covers a range larger than 45cm in all directions. This achieves a state-of-art energy-efficiency of 11pJ/bit. The 29mW/element power consumption also demonstrates the lowest power of a single phased-array element.

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