Cmos Test And Evaluation A Physical Perspective

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On IDDT Testing of CMOS Circuits for Stuck-open Faults
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ISTFA 2019: Proceedings of the 45th International Symposium for Testing and Failure Analysis
Scientific and Technical Aerospace Reports
Wafer Level Reliability of Advanced CMOS Devices and Processes
NASA Technical Paper
ESD Testing
Shortcomings in Ground Testing, Environment Simulations, and Performance Predictions for Space Applications
Iddq Testing for CMOS VLSI
Advances in Nonlinear Speech Processing
DCIS2002
Digital Circuit Testing and Testability
Developments in Integrated Circuit Testing
Microelectronic Test Structures for CMOS Technology
Technical Abstract Bulletin
Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits
Microelectronic Failure Analysis Desk Reference
Automatic Testing and Evaluation of Digital Integrated Circuits
Journal of Testing and Evaluation
Testing Static Random Access Memories
Testing of Digital Systems
Testing and Reliable Design of CMOS Circuits
Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits
Introduction to IDDQ Testing
Testing and Diagnosis of VLSI and ULSI
IDDQ Testing of VLSI Circuits
Rapid Reliability Assessment of VLSICs
Thirty-fourth International Symposium for Testing and Failure Analysis
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Models in Hardware Testing
Microelectronics Failure Analysis
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Principles of Testing Electronic Systems
Microelectronic Failure Analysis

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CMOS Electronics Springer Science & Business Media
Microelectronic Test Structures for CMOS Technology and Products addresses the basic concepts of the design of test structures for incorporation within test-vehicles, scribe-lines, and CMOS products. The role of test structures in the development and monitoring of CMOS technologies and products has become ever more important with the increased cost and complexity of development and manufacturing. In this timely volume, IBM scientists Manjul Bhushan and Mark Ketchen emphasize high speed characterization techniques for digital CMOS circuit applications and bridging between circuit performance and characteristics of MOSFETs and other circuit elements. Detailed examples are presented throughout, many of which are equally applicable to other microelectronic technologies as well. The authors' overarching goal is to provide students and technology practitioners alike a practical guide to the disciplined design and use of test structures that give unambiguous information on the parametrics and performance of digital CMOS technology.

On IDDT Testing of CMOS Circuits for Stuck-open Faults
Springer Science & Business Media
This volume contains a collection of papers presented at the NATO Advanced Study Institute on ·Testing and Diagnosis of VLSI and ULSI" held at Villa Olmo, Como (Italy) June 22 -July 3,1987. High Density technologies such as Very-Large Scale Integration (VLSI), Wafer Scale Integration (WSI) and the not-so-far promises of Ultra-Large Scale Integration (ULSI), have exasperated the problema associated with the testing and diagnosis of these devices and systema. Traditional techniques are fast becoming obsolete due to unique requirements such as limited controllability and observability, increasing execution complexity for test vector generation and high cost of fault simulation, to mention just a few. New approaches are imperative to achieve the highly sought goal of the • three months· turn around cycle time for a state-of-the-art computer chip. The importance of testing and diagnostic processes is of primary importance if costs must be kept at acceptable levels. The objective of this NATO-ASI was to present, analyze and discuss the various facets of testing and diagnosis with respect to both theory and practice. The contents of this volume reflect the diversity of approaches currently available to reduce test and diagnosis time. These approaches are described in a concise, yet clear way by renowned experts of the field. Their contributions are aimed at a wide readership: the uninitiated researcher will find the tutorial chapters very rewarding. The expert will be introduced to advanced techniques in a very comprehensive manner.

Microelectronics Fialure Analysis Desk Reference, Seventh Edition Artech House Publishers
Testing Static Random Access Memories covers testing of one of the important semiconductor memories types; it addresses testing of static random access memories (SRAMs), both single-port and multi-port. It contributes to the technical acknowledge needed by those involved in memory testing, engineers and researchers. The book begins with outlining the most popular SRAMs architectures. Then, the description of realistic fault models, based on defect injection and SPICE simulation, are introduced. Thereafter, high quality and low cost test patterns, as well as test strategies for single-port, two-port and any p-port SRAMs are presented, together with some preliminary test results showing the importance of the new tests in reducing DPM level. The impact of the port restrictions (e.g., read-only ports) on the fault models, tests, and test strategies is also discussed. Features: -Fault primitive based analysis of memory faults, -A complete framework of and classification memory faults, -A systematic way to develop optimal and high quality memory test algorithms, -A systematic way to develop test patterns for any multi-port SRAM, -Challenges and trends in embedded memory testing.
ISTFA 2019: Proceedings of the 45th International Symposium for Testing and Failure Analysis Springer Science & Business Media
Model based testing is the most powerful technique for testing hardware and software systems. Models in Hardware Testing describes the use of models at all the levels of hardware testing. The relevant fault models for nanoscaled CMOS technology are introduced, and their implications on fault simulation, automatic test pattern generation, fault diagnosis, memory testing and power aware testing are discussed. Models and the corresponding algorithms are considered with respect to the most recent state of the art, and they are put into a historical context by a concluding chapter on the use of physical fault models in fault tolerance.
Scientific and Technical Aerospace Reports Cambridge University Press
This book constitutes the proceedings of the 6th International Conference on Nonlinear Speech Processing, NOLISP 2013, held in Mons, Belgium, in June 2013. The 27 refereed papers included in this volume were carefully reviewed and selected from 34 submissions. The paper are organized in topical sections on speech and audio analysis; speech synthesis; speech-based biomedical applications; automatic speech recognition; and speech enhancement.
Wafer Level Reliability of Advanced CMOS Devices and Processes Springer
Power supply current monitoring to detect CMOS IC defects during production testing quietly laid down its roots in the mid-1970s. Both Sandia Labs and RCA in the United States and Philips Labs in the Netherlands practiced this procedure on their CMOS ICs. At that time, this practice stemmed simply from an intuitive sense that CMOS ICs showing abnormal quiescent power supply current (IDDQ) contained defects. Later, this intuition was supported by data and analysis in the 1980s by Levi (RACD,

Malaiya and Su (SUNY-Binghamton), Soden and Hawkins (Sandia Labs and the University of New Mexico), Jacomino and co-workers (Laboratoire d'Automatique de Grenoble), and Maly and co-workers (Carnegie Mellon University). Interest in IDDQ testing has advanced beyond the data reported in the 1980s and is now focused on applications and evaluations involving larger volumes of ICs that improve quality beyond what can be achieved by previous conventional means. In the conventional style of testing one attempts to propagate the logic states of the suspended nodes to primary outputs. This is done for all or most nodes of the circuit. For sequential circuits, in particular, the complexity of finding suitable tests is very high. In comparison, the IDDQ test does not observe the logic states, but measures the integrated current that leaks through all gates. In other words, it is like measuring a patient's temperature to determine the state of health. Despite perceived advantages, during the years that followed its initial announcements, skepticism about the practicality of IDDQ testing prevailed. The idea, however, provided a great opportunity to researchers. New results on test generation, fault simulation, design for testability, built-in self-test, and diagnosis for this style of testing have since been reported. After a decade of research, we are definitely closer to practice.

NASA Technical Paper
Springer Science & Business Media
The 2nd edition of defect oriented testing has been extensively updated. New chapters on Functional, Parametric Defect Models and Inductive fault Analysis and Yield Engineering have been added to provide a link between defect sources and yield. The chapter on RAM testing has been updated with focus on parametric and SRAM stability testing. Similarly, newer material has been incorporated in digital fault modeling and analog testing chapters. The strength of Defect Oriented Testing for nano-Metric CMOS VLSIs lies in its industrial relevance.

ESD Testing Springer Science & Business Media
Device testing represents the single largest manufacturing expense in the semiconductor industry, costing over $40 billion a year. The most comprehensive and wide ranging book of its kind, Testing of Digital Systems covers everything you need to know about this vitally important subject. Starting right from the basics, the authors take the reader through automatic test pattern generation, design for testability and built-in self-test of digital circuits before moving on to more advanced topics such as IDDQ testing, functional testing, delay fault testing, memory testing, and fault diagnosis. The book includes detailed treatment of the latest techniques including test generation for various fault models, discussion of testing techniques at different levels of integrated circuit hierarchy and a chapter on system-on-a-chip test synthesis. Written for students and engineers, it is both an excellent senior/graduate level textbook and a valuable reference.

Shortcomings in Ground Testing, Environment Simulations, and Performance Predictions for Space Applications
John Wiley & Sons
Developed by the Electronic Device Failure Analysis Society (EDFAS)

Publications Committee.
Iddq Testing for CMOS VLSI Springer Science & Business Media
This book discusses in detail the correlation between physical defects and logic faults, and shows you how Iddq testing locates these defects. The book provides planning guidelines and optimization methods and is illustrated with numerous examples ranging from simple circuits to extensive case studies.

Advances in Nonlinear Speech Processing Academic Press
The definition from SEMATECH of wafer level reliability test is: a methodology to assess the reliability impact of tools and processes by testing mechanism-specific test structures under accelerated conditions during device processing. Because wafer level reliability test is the accelerated test, it owns some different characters with common long time test in terms of failure mechanisms, test procedures, life time prediction, test structures design and so on. In this book, all items of wafer level reliability of CMOS devices and processes will be discussed. The purpose of this book is to provide a good and urgently need reference on MOS device reliability. The authors discuss how to enhance the veracity of lifetime prediction and the effects to degrade the veracity deeply. Finally, a discussion of the problems with wafer level reliability in terms of the engineering applications and research is given.

DCIS2002 John Wiley & Sons
Provides new or expanded coverage on the latest techniques for microelectronic failure analysis. The CD-ROM includes the complete content of the book in fully searchable Adobe Acrobat format. Developed by the Electronic Device Failure Analysis Society (EDFAS) Publications Committee
Digital Circuit Testing and Testability ASM International
The increasing application of integrated circuits in situations where high reliability is needed places a requirement on the manufacturer to use methods of testing to eliminate devices that may fail on service. One possible approach that is described in this book is to make precise electrical measurements that may reveal those devices more likely to fail. The measurements assessed are of analog circuit parameters which, based on a knowledge of failure mechanisms, may indicate a future failure. . To incorporate these tests into the functional listing of very large scale integrated circuits consideration has to be given to the sensitivity of the tests where small numbers of devices may be defective in a complex circuit. In addition the tests ideally should require minimal extra test time. A range of tests has been evaluated and compared with simulation used to assess the sensitivity of the measurements. Other work in the field is fully referenced at the end of each chapter. The team at Lancaster responsible for this book wish to thank the Alvey directorate and SERe for the necessary support and encouragement to publish our results. We would also like to thank John Henderson, recently retired from the British Telecom Research Laboratories, for his cheerful and enthusiastic encouragement. Trevor Ingham, now in New Zealand, is thanked for his early work on the project.

Developments in Integrated Circuit Testing ASM International
Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits (ICs). However, the increased complexity and nanometer-size features of modern ICs make them susceptible to manufacturing defects, as well as performance and quality issues. Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens/bridges, and design-for-manufacturing (DfM)-related rule violations. The book also addresses testing for small-delay defects (SDDs), which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing, including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on "alternative methods" that explores new metrics, top-off ATPG, and circuit topology-based solutions Highlights the advantages and disadvantages of a diverse set of metrics, and identifies scope for improvement Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions.
Microelectronic Test Structures for CMOS Technology CRC Press
An easy to use introduction to the practices and techniques in the field of digital circuit testing. Lala writes in a user-friendly and tutorial style, making the book easy to read, even for the newcomer to fault-tolerant system design. Each informative chapter is self-contained, with little or no previous knowledge of a topic assumed. Extensive references follow each chapter.

Technical Abstract Bulletin ASM International
CMOS Test and Evaluation: A Physical Perspective is a single source for an integrated view of test and data analysis methodology for CMOS products, covering circuit sensitivities to MOSFET characteristics, impact of silicon technology process variability, applications of embedded test structures and sensors, product yield, and reliability over the lifetime of the product. This book also covers statistical data analysis and visualization techniques, test equipment and CMOS product specifications, and examines product behavior over its full voltage, temperature and frequency range.
Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits Springer Science & Business Media
CMOS manufacturing environments are surrounded with symptoms that can indicate serious test, design, or reliability problems, which, in turn, can affect the financial as well as the engineering bottom line. This book educates readers, including non-engineers involved in CMOS

manufacture, to identify and remedy these causes. This book instills the electronic knowledge that affects not just design but other important areas of manufacturing such as test, reliability, failure analysis, yield-quality issues, and problems. Designed specifically for the many non-electronic engineers employed in the semiconductor industry who need to reliably manufacture chips at a high rate in large quantities, this is a practical guide to how CMOS electronics work, how failures occur, and how to diagnose and avoid them. Key features: Builds a grasp of the basic electronics of CMOS integrated circuits and then leads the reader further to understand the mechanisms of failure. Unique descriptions of circuit failure mechanisms, some found previously only in research papers and others new to this publication. Targeted to the CMOS industry (or students headed there) and not a generic introduction to the broader field of electronics. Examples, exercises, and problems are provided to support the self-instruction of the reader.

Microelectronic Failure Analysis Desk Reference ASM International
The theme for the 2019 conference is Novel Computing Architectures. Papers will include discussions on the advent of Artificial Intelligence and the promise of quantum computing that are driving disruptive computing architectures; Neuromorphic chip designs on one hand, and Quantum Bits on the other, still in R&D, will introduce new computing circuitry and memory elements, novel materials, and different test methodologies. These novel computing architectures will require further innovation which is best achieved through a collaborative Failure Analysis community composed of chip manufacturers, tool vendors, and universities.

Automatic Testing and Evaluation of Digital Integrated Circuits
Springer
The Electronic Device Failure Analysis Society proudly announces the Seventh Edition of the Microelectronics Failure Analysis Desk Reference, published by ASM International. The new edition will help engineers improve their ability to verify, isolate, uncover, and identify the root cause of failures. Prepared by a team of experts, this updated reference offers the latest information on advanced failure analysis tools and techniques, illustrated with numerous real-life examples. This book is geared to practicing engineers and for studies in the major area of power plant engineering. For non-metallurgists, a chapter has been devoted to the basics of material science, metallurgy of steels, heat treatment, and structure-property correlation. A chapter on materials for boiler tubes covers composition and application of different grades of steels and high temperature alloys currently in use as boiler tubes and future materials to be used in supercritical, ultra-supercritical and advanced ultra-supercritical thermal power plants. A comprehensive discussion on different mechanisms of boiler tube failure is the heart of the book. Additional chapters detailing the role of advanced material characterization techniques in failure investigation and the role of water chemistry in tube failures are key

contributions to the book.
Journal of Testing and Evaluation ASM International
Este libro contiene las presentaciones de la XVII Conferencia de Diseño de Circuitos y Sistemas Integrados celebrado en el Palacio de la Magdalena, Santander, en noviembre de 2002. Esta Conferencia ha alcanzado un alto nivel de calidad, como consecuencia de su tradición y madurez, que lo convierte en uno de los acontecimientos más importantes para los circuitos de microelectrónica y la comunidad de diseño de sistemas en el sur de Europa. Desde su origen tiene una gran contribución de Universidades españolas, aunque hoy los autores participan desde catorce países

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