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instruction to memory. Why is this difficult to do? It is difficult to UNDO the effect of a store instruction. Another processor might read and use the value supplied by the store instruction before the store is undone.

EXAM 1 SOLUTIONS

solution of computer architecture

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1. Stalls and performance • Stalls impede progress of a pipeline and result in deviation from 1 instruction executing/clock cycle •

CPI pipelined = - Ideal CPI + Pipeline stall cycles per instruction - 1 + Pipeline stall cycles per instruction • Ignoring overhead and assuming stages are

balanced: • Ideally, speedup equal to # of ...Computer Architecture Exercises with Solutions

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EXAM 1 SOLUTIONS

Assume we would like
to use the exact same
solution (history buffer)
for executing a store
instruction to memory.

Why is this difficult to
do? It is difficult to

UNDO the effect of a
store instruction.

Another processor

might read and use the value supplied by the store instruction before the store is undone.

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COE818 Advanced Computer Architecture Midterm Test Solutions 3 Question # 1.3

Calculate how many clock cycles will take execution of this segment on the simple pipeline with normal forwarding and bypassing when result of branch instruction (new PC content) is available after completion of the ID stage.

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executing/clock cycle •

CPI pipelined = - Ideal

CPI + Pipeline stall

cycles per instruction -

1 + Pipeline stall cycles

per instruction •

Ignoring overhead and assuming stages are balanced: • Ideally,

speedup equal to # of ...

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