Clock Domain Crossing University Of Florida

Tom's Midnight Garden
Design, Verification and Testing
Proceedings : 19-23 April, Crete, Greece
RTL Hardware Design Using VHDL
Assertion-Based Design
Digital Systems Engineering
Proceedings of the joint Workshop on Sustained Simulation Performance, University of Stuttgart (HLRS) and Tohoku University, 2014
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10th International Symposium on Asynchronous Circuits and Systems
Advanced FPGA Design
Hardware Implementation and Correctness Proof
Power and Timing Modeling, Optimization and Simulation; 14th International Workshop, PATMOS 2004, Santorini, Greece, September 15-17, 2004, Proceedings
Digital Design

Sustained Simulation Performance 2014
Architecture, Implementation, and Optimization
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The Art of Hardware Architecture
DSP for Embedded and Real-Time Systems
Using Synopsys® Design CompilerTM and PrimeTime®
Issues in Nuclear and Plasma Science and Technology: 2012 Edition
Coding for Efficiency, Portability, and Scalability
SWE
Proceedings of the 3rd International Conference on Communication, Devices and Computing
Proceedings
Hot Interconnects : Proceedings : 20-22 August 2003, Stanford University, Stanford, California, USA
VLSI-SoC: System-on-Chip in the Nanoscale Era – Design, Verification and Reliability

LACEY BURGESS

Tom's Midnight Garden ScholarlyEditions
Provides students with a system-level perspective and the tools they need to understand, analyze and design complete digital systems using Verilog. It goes beyond the design of simple combinational and sequential modules to show how such modules are used to build complete systems, reflecting digital design in the real world.
Design, Verification and Testing Springer Science & Business Media
The skills and guidance needed to master RTL hardware design

This book teaches readers how to systematically design efficient,portable, and scalable Register Transfer Level (RTL) digitalcircuits using the VHDL hardware description language and synthesissoftware. Focusing on the module-level design, which is composed offunctional units, routing circuit, and storage, the bookillustrates the relationship between the VHDL constructs and theunderlying hardware components, and shows how to develop codes thatfaithfully reflect the module-level design and can be synthesizedinto efficient gate-level implementation. Several unique features distinguish the book: * Coding style that shows a clear relationship between VHDLconstructs and hardware components * Conceptual diagrams that illustrate the realization of VHDLcodes * Emphasis on the code reuse * Practical examples that demonstrate and reinforce designconcepts, procedures, and

techniques * Two chapters on realizing sequential algorithms in hardware * Two chapters on scalable and parameterized designs andcoding * One chapter covering the synchronization and interface betweenmultiple clock domains Although the focus of the book is RTL synthesis, it also examinesthe synthesis task from the perspective of the overall developmentprocess. Readers learn good design practices and guidelines toensure that an RTL design can accommodate future simulation,verification, and testing needs, and can be easily incorporatedinto a larger system or reused. Discussion is independent oftechnology and can be applied to both ASIC and FPGA devices. With a balanced presentation of fundamentals and practicalexamples, this is an excellent textbook for upper-levelundergraduate or graduate courses in advanced digital logic.Engineers who need to make effective use of today's synthesissoftware and FPGA devices should also refer to this book.

Proceedings : 19-23 April, Crete, Greece John Wiley & Sons

Create low power, higher performance circuits with shorter design times using this practical guide to asynchronous design. This practical alternative to conventional synchronous design enables performance close to full-custom designs with design times that approach commercially available ASIC standard cell flows. It includes design trade-offs, specific design examples, and end-of-chapter exercises. Emphasis throughout is placed on practical techniques and real-world applications, making this ideal for circuit design students interested in alternative design styles and system-on-chip circuits, as well as circuit designers in industry who need new solutions to old problems.

RTL Hardware Design Using VHDL Springer Science & Business Media

Design and Verification of Clock Domain Crossing InterfacesA Digital Signal Processor for Particle DetectorsDesign, Verification and TestingSpringer Nature

Assertion-Based Design Springer

This book provides a hands-on, application-oriented guide to the entire IEEE standard 1800 SystemVerilog language. Readers will benefit from the step-by-step approach to learning the language and methodology nuances, which will enable them to design and verify complex ASIC/SoC and CPU chips. The author covers the entire spectrum of the language, including random constraints, SystemVerilog Assertions, Functional Coverage, Class, checkers, interfaces, and Data Types, among other features of the language. Written by an experienced, professional end-user of ASIC/SoC/CPU and FPGA designs, this book explains each concept with easy to understand examples, simulation logs and applications derived from real projects. Readers will be empowered to tackle the complex task of multi-million gate ASIC designs. Provides comprehensive coverage of the entire IEEE standard SystemVerilog language; Covers important topics such as constrained random verification, SystemVerilog Class, Assertions, Functional coverage, data types, checkers, interfaces, processes and procedures, among other language features; Uses easy to understand examples and simulation logs; examples are simulatable and will be provided online; Written by an experienced, professional end-user of ASIC/SoC/CPU and FPGA designs. This is quite a comprehensive work. It must have taken a long time to write it. I really like that the author has taken apart each of the SystemVerilog constructs and talks about them in

great detail, including example code and simulation logs. For example, there is a chapter dedicated to arrays, and another dedicated to queues - that is great to have! The Language Reference Manual (LRM) is quite dense and difficult to use as a text for learning the language. This book explains semantics at a level of detail that is not possible in an LRM. This is the strength of the book. This will be an excellent book for novice users and as a handy reference for experienced programmers. Mark Glasser Cerebras Systems

Digital Systems Engineering Springer Science & Business Media

This book constitutes the refereed proceedings of the 14th International Workshop on Power and Timing Optimization and Simulation, PATMOS 2004, held in Santorini, Greece in September 2004. The 85 revised papers presented together with abstracts of 6 invited presentations were carefully reviewed and selected from 152 papers submitted. The papers are organized in topical sections on buses and communication, circuits and devices, low power issues, architectures, asynchronous circuits, systems design, interconnect and physical design, security and safety, low-power processing, digital design, and modeling and simulation.

Proceedings of the joint Workshop on Sustained Simulation Performance, University of Stuttgart (HLRS) and Tohoku University, 2014 Springer

What makes some computers slow? Why do some digital systems operate reliably for years while others fail mysteriously every few hours? How can some systems dissipate kilowatts while others operate off batteries? These questions of speed, reliability, and power are all determined by the system-level electrical design of a digital system. Digital Systems Engineering presents a comprehensive treatment of these topics. It combines a rigorous development of the fundamental principles in each area with real-world examples of circuits and methods. The book not only serves as an undergraduate textbook, filling the gap between circuit design and logic design, but can also help practising digital designers keep pace with the speed and power of modern integrated circuits. The techniques described in this book, once used only in supercomputers, are essential to the correct and efficient operation of any type of digital system.

Embedded Computer Systems: Architectures, Modeling, and Simulation Springer Science & Business Media

This book describes in detail all required technologies and methodologies needed to create a comprehensive, functional design verification strategy and environment to tackle the toughest job of guaranteeing first-pass working silicon. The author first outlines all of the verification sub-fields at a high level, with just enough depth to allow an engineer to grasp the field before delving into its detail. He then describes in detail industry standard technologies such as UVM (Universal Verification Methodology), SVA (SystemVerilog Assertions), SFC (SystemVerilog Functional Coverage), CDV (Coverage Driven Verification), Low Power Verification (Unified Power Format UPF), AMS (Analog Mixed Signal) verification, Virtual Platform TLM2.0/ESL (Electronic System Level) methodology, Static Formal Verification, Logic Equivalency Check (LEC), Hardware Acceleration, Hardware Emulation, Hardware/Software Co-verification, Power Performance Area (PPA) analysis on a virtual

platform, Reuse Methodology from Algorithm/ESL to RTL, and other overall methodologies.

A Designer's Guide to Asynchronous VLSI Springer Nature
This book provides insights into the 3rd International Conference on Communication, Devices and Computing (ICCDC 2021), which was held in Haldia, India, on August 1618, 2021. It covers new ideas, applications, and the experiences of research engineers, scientists, industrialists, scholars, and students from around the globe. The proceedings highlight cutting-edge research on communication, electronic devices, and computing and address diverse areas such as 5G communication, spread spectrum systems, wireless sensor networks, and signal processing for secure communication, error control coding, printed antennas, analysis of wireless networks, antenna array systems, analog and digital signal processing for communication systems, frequency selective surfaces, radar communication, and substrate integrated waveguide and microwave passive components, which are key to state-of-the-art innovations in communication technologies. .

11th Symposium on High Performance Interconnects Cambridge University Press
This book highlights the complex issues, tasks and skills that must be mastered by an IP designer, in order to design an optimized and robust digital circuit to solve a problem. The techniques and methodologies described can serve as a bridge between specifications that are known to the designer and RTL code that is final outcome, reducing significantly the time it takes to convert initial ideas and concepts into right-first-time silicon. Coverage focuses on real problems rather than theoretical concepts, with an emphasis on design techniques across various aspects of chip-design.

Advanced ASIC Chip Synthesis Springer
This monograph is based on the third author's lectures on computer architecture, given in the summer semester 2013 at Saarland University, Germany. It contains a gate level construction of a multi-core machine with pipelined MIPS processor cores and a sequentially consistent shared memory. The book contains the first correctness proofs for both the gate level implementation of a multi-core processor and also of a cache based sequentially consistent shared memory. This opens the way to the formal verification of synthesizable hardware for multi-core processors in the future. Constructions are in a gate level hardware model and thus deterministic. In contrast the reference models against which correctness is shown are nondeterministic. The development of the additional machinery for these proofs and the correctness proof of the shared memory at the gate level are the main technical contributions of this work.

Software System Reliability and Security Evgeni Stavinov
The SAMOS workshop is an international gathering of highly quali?ed researchers from academia and industry, sharing in a 3-day lively discussion on the quiet and - spiring northern mountainside of the Mediterranean island of Samos. As a tradition, the workshop features workshop presentations in the morning, while after lunch all kinds of informal discussions and nut-cracking gatherings take place. The workshop is unique in the sense that not only solved research problems are presented and discussed but also (partly) unsolved problems and in-depth topical reviews can be unleashed in the sci- ti?c arena.

Consequently, the workshop provides the participants with an environment where collaboration rather than competition is fostered. The earlier workshops, SAMOS I–IV (2001–2004), were composed only of invited presentations. Due to increasing expressions of interest in the workshop, the Program Committee of SAMOS V decided to open the workshop for all submissions. As a result the SAMOS workshop gained an immediate popularity; a total of 114 submitted papers were received for evaluation. The papers came from 24 countries and regions: Austria (1), Belgium (2), Brazil (5), Canada (4), China (12), Cyprus (2), Czech Republic (1), Finland (15), France (6), Germany (8), Greece (5), Hong Kong (2), India (2), Iran (1), Korea (24), The Netherlands (7), Pakistan (1), Poland (2), Spain (2), Sweden (2), T- wan (1), Turkey (2), UK (2), and USA (5). We are grateful to all of the authors who submitted papers to the workshop.

Nanometer Design for Testability Springer

Today’s networks of processors on and off chip, operating with independent clocks, need effective synchronization of the data passing between them for reliability. When two or more processors request access to a common resource, such as a memory, an arbiter has to decide which request to deal with first. Current developments in integrated circuit processing are leading to an increase in the numbers of independent digital processing elements in a single system. With this comes faster communications, more networks on chip, and the demand for more reliable, more complex, and higher performance synchronizers and arbiters. Written by one of the foremost researchers in this area of digital design, this authoritative text provides in-depth theory and practical design solutions for the reliable working of synchronization and arbitration hardware in digital systems. The book provides methods for making real reliability measurements both on and off chip, evaluating some of the common difficulties and detailing circuit solutions at both circuit and system levels. Synchronization and Arbitration in Digital Systems also presents: mathematical models used to estimate mean time between failures in digital systems; a summary of serial and parallel communication techniques for on-chip data transmission; explanations on how to design a wrapper for a locally synchronous cell, highlighting the issues associated with stoppable clocks; an examination of various types of priority arbiters, using signal transition graphs to show the specification of different designs (from the simplest to more complex multi-way arbiters) including ways of solving problems encountered in a wide range of applications; essential information on systems composed of independently timed regions, including a discussion on the problem of choice and the factors affecting the time taken to make choices in electronics. With its logical approach to design methodology, this will prove an invaluable guide for electronic and computer engineers and researchers working on the design of digital electronic hardware. Postgraduates and senior undergraduate students studying digital systems design as part of their electronic engineering course will struggle to find a resource that better details the information given inside this book Springer

Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased

performance-capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost. This book is a comprehensive guide to new VLSI Testing and Design-for-Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly System-on-Chip Test architectures, for test debug and diagnosis of digital, memory, and analog/mixed-signal designs. Emphasizes VLSI Test principles and Design for Testability architectures, with numerous illustrations/examples. Most up-to-date coverage available, including Fault Tolerance, Low-Power Testing, Defect and Error Tolerance, Network-on-Chip (NOC) Testing, Software-Based Self-Testing, FPGA Testing, MEMS Testing, and System-In-Package (SIP) Testing, which are not yet available in any testing book. Covers the entire spectrum of VLSI testing and DFT architectures, from digital and analog, to memory circuits, and fault diagnosis and self-repair from digital to memory circuits. Discusses future nanotechnology test trends and challenges facing the nanometer design era; promising nanotechnology test techniques, including Quantum-Dots, Cellular Automata, Carbon-Nanotubes, and Hybrid Semiconductor/Nanowire/Molecular Computing. Practical problems at the end of each chapter for students.

5th International Workshop, SAMOS 2005, Samos, Greece, July 18-20, Proceedings John Wiley & Sons

"Tom is not prepared for what is about to happen when he hears the grandfather clock strike thirteen. Outside the back door is a garden, which everyone tells him does not exist."--Page 4 de la couverture.

A Digital Signal Processor for Particle Detectors John Wiley & Sons

This book presents the state of the art in high-performance computing and simulation on modern supercomputer architectures. It covers trends in hardware and software development in general and the future of high-performance systems and heterogeneous architectures in particular. The application-related contributions cover computational fluid dynamics, material science, medical applications and climate research; innovative fields such as coupled multi-physics and multi-scale simulations are highlighted. All papers were chosen from presentations given at the 18th Workshop on Sustained Simulation Performance held at the HLRS, University of Stuttgart, Germany in October 2013 and subsequent Workshop of the same name held at Tohoku University in March 2014.

Selected Contributions from FDL 2015 Springer Nature

As Moore’s law continues to unfold, two important trends have recently emerged. First, the growth of chip capacity is translated into a corresponding increase of number of cores. Second, the parallelization of the computation and 3D integration technologies lead to distributed memory architectures. This book describes recent research that addresses urgent challenges in many-core architectures and application mapping. It addresses the architectural design of many core chips, memory and data management, power management, design and programming methodologies. It also describes how new techniques have been applied in various industrial case studies.

The Phantom Tollbooth Design and Verification of Clock Domain Crossing InterfacesA Digital Signal Processor for Particle DetectorsDesign, Verification and Testing

This book provides the advanced issues of FPGA design as the underlying theme of the work. In practice, an engineer typically needs to be mentored for several years before these principles are appropriately utilized. The topics that will be discussed in this book are essential to designing FPGA's beyond moderate complexity. The goal of the book is to present practical design techniques that are otherwise only available through mentorship and real-world experience.

Languages, Design Methods, and Tools for Electronic System Design Springer Science & Business Media

This Expert Guide gives you the techniques and technologies in digital signal processing (DSP) to optimally design and implement your embedded system. Written by experts with a solutions focus, this encyclopedic reference gives you an indispensable aid to tackling the day-to-day problems you face in using DSP to develop embedded systems. With this book you will learn: A range of development techniques for developing DSP code Valuable tips and tricks for optimizing DSP software for maximum performance The various options available for constructing DSP systems from numerous software components The tools available for developing DSP applications Numerous practical guidelines from experts with wide and lengthy experience of DSP application development Features: Several areas of research being done in advanced DSP technology Industry case studies on DSP systems development DSP for Embedded and Real-Time Systems is the reference for both the beginner and experienced, covering most aspects of using today's DSP techniques and technologies for designing and implementing an optimal embedded system. The only complete reference which explains all aspects of using DSP in embedded systems development making it a rich resource for every day use Covers all aspects of using today's DSP techniques and technologies for designing and implementing an optimal embedded system Enables the engineer to find solutions to all the problems they will face when using DSP

Integrated Circuit and System Design Yearling Books

This book is designed to serve as a hands-on professional reference with additional utility as a textbook for upper undergraduate and some graduate courses in digital logic design. This book is organized in such a way that that it can describe a number of RTL design scenarios, from simple to complex. The book constructs the logic design story from the fundamentals of logic design to advanced RTL design concepts. Keeping in view the importance of miniaturization today, the book gives practical information on the issues with ASIC RTL design and how to overcome these concerns. It clearly explains how to write an efficient RTL code and how to improve design performance. The book also describes advanced RTL design concepts such as low-power design, multiple clock-domain design, and SOC-based design. The practical orientation of the book makes it ideal for training programs for practicing design engineers and for short-term vocational programs. The contents of the book will also make it a useful read for students and hobbyists.

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