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BLAINE ARIANA

The Designer’s Guide to Verilog-AMS Springer Science & Business Media
Based on the highly successful second edition, this extended edition of SystemVerilog for Verification: A Guide to Learning the Testbench Language Features teaches all verification features of the SystemVerilog language, providing hundreds of examples to clearly explain the concepts and basic fundamentals. It contains materials for both the full-time verification engineer and the student learning this valuable skill. In the third edition, authors Chris Spear and Greg Tumbush start with how to verify a design, and then use that context to demonstrate the language features, including the advantages and disadvantages of different styles, allowing readers to choose between alternatives. This textbook contains end-of-chapter exercises designed to enhance students’ understanding of the material. Other features of this revision include: New sections on static variables, print specifiers, and DPI from the 2009 IEEE language standard Descriptions of UVM features such as factories, the test registry, and the configuration database Expanded code samples and explanations Numerous samples that have been tested on the major SystemVerilog simulators SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Third Edition is suitable for use in a one-semester SystemVerilog course on SystemVerilog at the undergraduate or graduate level. Many of the improvements to this new edition were compiled through feedback provided from hundreds of readers.
12th Annual IEEE Symposium on Field-Programmable Custom Computing Machines : Proceedings : 20-23 April, 2004, Napa, California Springer Science & Business Media
"BSV (Bluespec System Verilog) is a language used in the design of electronic systems (ASIC's, FPGA's and systems)" -- P. 13.
Understanding the Linux Kernel Springer Science & Business Media
Are you an RTL or system designer that is currently using, moving, or planning to move to an HLS design environment? Finally, a comprehensive guide for designing hardware using C++ is here. Michael Fingeroff's High-Level Synthesis Blue Book presents the most effective C++ synthesis coding style for achieving high quality RTL. Master a totally new design methodology for coding increasingly complex designs! This book provides a step-by-step approach to using C++ as a hardware design language, including an introduction to the basics of HLS using concepts familiar to RTL designers. Each chapter provides easy-to-understand C++ examples, along with hardware and timing diagrams where appropriate. The book progresses from simple concepts such as sequential logic design to more complicated topics such as memory architecture and hierarchical sub-system design. Later chapters bring together many of the earlier HLS design concepts through their application in simplified design examples. These examples illustrate the fundamental principles behind C++ hardware design, which will translate to much larger designs. Although this book focuses primarily on C and C++ to present the basics of C++ synthesis, all of the concepts are equally applicable to SystemC when describing the core algorithmic part of a design. On completion of this book, readers should be well on their way to becoming experts in high-level synthesis.
From Algorithm to Chip with Verilog MIT Press

The Definitive, Up-to-Date Guide to Digital Design with SystemVerilog: Concepts, Techniques, and Code To design state-of-the-art digital hardware, engineers first specify functionality in a high-level Hardware Description Language (HDL)—and today's most powerful, useful HDL is SystemVerilog, now an IEEE standard. Digital System Design with SystemVerilog is the first comprehensive introduction to both SystemVerilog and the contemporary digital hardware design techniques used with it. Building on the proven approach of his bestselling Digital System Design with VHDL, Mark Zwolinski covers everything engineers need to know to automate the entire design process with SystemVerilog—from modeling through functional simulation, synthesis, timing simulation, and verification. Zwolinski teaches through about a hundred and fifty practical examples, each with carefully detailed syntax and enough in-depth information to enable rapid hardware design and verification. All examples are available for download from the book's companion Web site, zwolinski.org. Coverage includes Using electronic design automation tools with programmable logic and ASIC technologies Essential principles of Boolean algebra and combinational logic design, with discussions of timing and hazards Core modeling techniques: combinational building blocks, buffers, decoders, encoders, multiplexers, adders, and parity checkers Sequential building blocks: latches, flip- flops, registers, counters, memory, and sequential multipliers Designing finite state machines: from ASM chart to D flip-flops, next state, and output logic Modeling interfaces and packages with SystemVerilog Designing testbenches: architecture, constrained random test generation, and assertion-based verification Describing RTL and FPGA synthesis models Understanding and implementing Design-for-Test Exploring anomalous behavior in asynchronous sequential circuits Performing Verilog-AMS and mixed-signal modeling Whatever your experience with digital design, older versions of Verilog, or VHDL, this book will help you discover SystemVerilog's full power and use it to the fullest.

Theory and Design (with VHDL and SystemVerilog) Springer Science & Business Media

XV From the Old to the New xvii Acknowledgments xx| Verilog A Tutorial Introduction Getting Started 2 A Structural Description 2 Simulating the binaryToESeg Driver 4 Creating Ports For the Module 7 Creating a Testbench For a Module 8 Behavioral Modeling of Combinational Circuits 11 Procedural Models 12 Rules for Synthesizing Combinational Circuits 13 Procedural Modeling of Clocked Sequential Circuits 14 Modeling Finite State Machines 15 Rules for Synthesizing Sequential Systems 18 Non-Blocking Assignment ("

100 Power Tips for FPGA Designers Morgan & Claypool Publishers

mental improvements during the same period. What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough. In the second edition of Writing Testbenches, Bergeron raises the verification level of abstraction by introducing coverage-driven constrained-random transaction-level self-checking testbenches all made possible through the introduction of hardware verification languages (HVLs), such as e from Verisity and OpenVera from Synopsys. The state-of-art methodologies described in Writing Test benches will contribute greatly to the much-needed equivalent of a synthesis breakthrough in verification productivity. I not only highly recommend this book, but also I think it should be required reading by anyone involved in design and verification of today's ASIC, SoCs and systems. Harry Foster Chief Architect Verplex Systems, Inc. xviii Writing Testbenches: Functional Verification of HDL Models PREFACE If you survey hardware design groups, you will learn that between 60% and 80% of their effort is now dedicated to verification.

The Next-generation Language for Electronic System Design Springer Science & Business Media

This book will help engineers write better Verilog/SystemVerilog design and verification code as well as deliver digital designs to market more quickly. It shows over 100 common coding mistakes that can be made with the Verilog and SystemVerilog languages. Each example explains in detail the symptoms of the error, the languages rules that cover the error, and the correct coding style to avoid the error. The book helps digital design and verification engineers to recognize, and avoid, these common coding mistakes. Many of these errors are very subtle, and can potentially cost hours or days of lost engineering time trying to find and debug them.

The Verilog PLI Handbook Springer

This book provides comprehensive coverage of 3D vision systems, from vision models and state-of-the-art algorithms to their hardware architectures for implementation on DSPs, FPGA and ASIC chips, and GPUs. It aims to fill the gaps between computer vision algorithms and real-time digital circuit implementations, especially with Verilog HDL design. The organization of this book is vision and hardware module directed, based on Verilog vision modules, 3D vision modules, parallel vision architectures, and Verilog designs for the stereo matching system with various parallel architectures. Provides Verilog vision simulators, tailored to the design and testing of general vision chips Bridges the differences between C/C++ and HDL to encompass both software realization and chip implementation; includes numerous examples that realize vision algorithms and general vision processing in HDL Unique in providing an organized and complete overview of how a real-time 3D vision system-on-chip can be designed Focuses on the digital VLSI aspects and implementation of digital signal processing tasks on hardware platforms such as ASICs and FPGAs for 3D vision systems, which have not been comprehensively covered in one single book Provides a timely view of the pervasive use of vision systems and the challenges of fusing information from different vision modules Accompanying website includes software and HDL code packages to enhance further learning and develop advanced systems A solution set and lecture slides are provided on the book's companion website The book is aimed at graduate students and researchers in computer vision and embedded systems, as well as chip and FPGA designers. Senior undergraduate students specializing in VLSI design or computer vision will also find the book to be helpful in understanding advanced applications.

Convergence and Hybrid Information Technology John Wiley & Sons

Quickly Engages in Applying Algorithmic Techniques to Solve Practical Signal Processing Problems With its active, hands-on learning approach, this text enables readers to master the underlying principles of digital signal processing and its many applications in industries such as digital television, mobile and broadband communications, and medical/scientific devices. Carefully developed MATLAB® examples throughout the text illustrate the mathematical concepts and use of digital signal processing algorithms. Readers will develop a deeper understanding of how to apply the algorithms by manipulating the codes in the examples to see their effect. Moreover, plenty of exercises help to put knowledge into practice solving real-world signal processing challenges. Following an introductory chapter, the text explores: Sampled signals and digital processing Random signals Representing signals and systems Temporal and spatial signal processing Frequency analysis of signals Discrete-time filters and recursive filters Each chapter begins with chapter objectives and an introduction. A summary at the end of each chapter ensures that one has mastered all the key concepts and techniques before progressing in the text. Lastly, appendices listing selected web resources, research papers, and related textbooks enable the investigation of individual topics in greater depth. Upon completion of this text, readers will understand how to apply key algorithmic techniques to address practical signal processing problems as well as develop their own signal processing algorithms. Moreover, the text provides a solid foundation for evaluating and applying new digital processing signal techniques as they are developed.

A User's Guide and Comprehensive Reference on the Verilog Programming Language Interface Cengage Learning

The Verilog hardware description language (HDL) provides the ability to describe digital and analog systems. This ability spans the range from descriptions that express conceptual and architectural design to detailed descriptions of implementations in gates and transistors. Verilog was developed originally at Gateway Design Automation Corporation during the mid-eighties. Tools to verify designs expressed in Verilog were implemented at the same time and marketed. Now Verilog is an open standard of IEEE with the number 1364. Verilog HDL is now used universally for digital designs in ASIC, FPGA, microprocessor, DSP and many other kinds of design-centers and is supported by most of the EDA companies. The research and education that is conducted in many universities is also using Verilog. This book introduces the Verilog hardware description language and describes it in a comprehensive manner. Verilog HDL was originally developed and specified with the intent of use with a simulator. Semantics of the language had not been fully described until now. In this book, each feature of the language is described using semantic introduction, syntax and examples. Chapter 4 leads to the full semantics of the language by providing definitions of terms, and explaining data structures and algorithms. The book is written with the approach that Verilog is not only a simulation or synthesis language, or a formal method of describing design, but a complete language addressing all of these aspects. This book covers many aspects of Verilog HDL that are essential parts of any design process.

SystemVerilog for Verification Institute of Electrical & Electronics Engineers(IEEE)

Starts with an overview of today's FPGA technology, devices, and tools for designing state-of-the-art DSP systems. A case study in the first chapter is the basis for more than 30 design examples throughout. The following chapters deal with computer arithmetic concepts, theory and the implementation of FIR and IIR filters, multirate digital signal processing systems, DFT and FFT algorithms, and advanced algorithms with high future potential. Each chapter contains exercises. The VERILOG source code and a glossary are given in the appendices, while the accompanying CD-ROM contains the examples in VHDL and Verilog code as well as the newest Altera "Baseline" software. This edition has a new chapter on adaptive filters, new sections on division and floating point arithmetics, an up-date to the current Altera software, and some new exercises.

Introduction to Logic Circuits & Logic Design with Verilog Xlibris Corporation

FPGA Prototyping Using Verilog Examples will provide you with a hands-on introduction to Verilog synthesis and FPGA programming through a "learn by doing" approach. By following the clear, easy-to-understand templates for code development and the numerous practical examples, you can quickly develop and simulate a sophisticated digital circuit, realize it on a prototyping device, and verify the operation of its physical implementation. This introductory text that will provide you with a solid foundation, instill confidence with rigorous examples for complex systems and prepare you for future development tasks.

FCCM 2004 Convergence and Hybrid Information Technology5th International Conference, ICHIT 2011, Daejeon, Korea, September 22-24, 2011, Proceedings

Most of the recent texts on compact modeling are limited to a particular class of semiconductor devices and do not provide comprehensive coverage of the field. Having a single comprehensive reference for the compact models of most commonly used semiconductor devices (both active and passive) represents a significant advantage for the reader. Indeed, several kinds of semiconductor devices are routinely encountered in a single IC design or in a single modeling support group. Compact Modeling includes mostly the material that after several years of IC design applications has been found both theoretically sound and practically significant. Assigning the individual chapters to the groups responsible for the definitive work on the subject assures the highest possible degree of expertise on each of the covered models.

Verilog HDL Springer Science & Business Media

A comprehensive guide to the theory and design of hardware-implemented finite state machines, with design examples developed in both VHDL and SystemVerilog languages. Modern, complex digital systems invariably include hardware-implemented finite state machines. The correct design of such parts is crucial for attaining proper system performance. This book offers detailed, comprehensive coverage of the theory and design for any category of hardware-implemented finite state machines. It describes crucial design problems that lead to incorrect or far from optimal implementation and provides examples of finite state machines developed in both VHDL and SystemVerilog (the successor of Verilog) hardware description languages. Important features include: extensive review of design practices for sequential digital circuits; a new division of all state machines into three hardware-based categories, encompassing all possible situations, with numerous practical examples provided in all three categories; the presentation of complete designs, with detailed VHDL and SystemVerilog codes, comments, and simulation results, all tested in FPGA devices; and exercise examples, all of which can be synthesized, simulated, and physically implemented in FPGA boards. Additional material is available on the book's Website. Designing a state machine in hardware is more complex than designing it in software. Although interest in hardware for finite state machines has grown dramatically in recent years, there is no comprehensive treatment of the subject. This book offers the most detailed coverage of finite state machines available. It will be essential for industrial designers of digital systems and for students of electrical engineering and computer science.

Digital System Design with SystemVerilog John Wiley & Sons

This textbook for courses in Digital Systems Design introduces students to the fundamental hardware used in modern computers. Coverage includes both the classical approach to digital system design (i.e., pen and paper) in addition to the modern hardware description language (HDL) design approach (computer-based). Using this textbook enables readers to design digital systems using the modern HDL approach, but they have a broad foundation of knowledge of the underlying hardware and theory of their designs. This book is designed to match the way the material is actually taught in the classroom. Topics are presented in a manner which builds foundational knowledge before moving onto advanced topics. The author has designed the presentation with learning goals and assessment at its core. Each section addresses a specific learning outcome that the student should be able to "do" after its completion. The concept checks and exercise problems provide a rich set of assessment tools to measure student performance on each outcome.

Digital Design with Chisel Springer Science & Business Media

FPGAs have almost entirely replaced the traditional Application Specific Standard Parts (ASSP) such

as the 74xx logic chip families because of their superior size, versatility, and speed. For example, FPGAs provide over a million fold increase in gates compared to ASSP parts. The traditional approach for hands-on exercises has relied on ASSP parts, primarily because of their simplicity and ease of use for the novice. Not only is this approach technically outdated, but it also severely limits the complexity of the designs that can be implemented. By introducing the readers to FPGAs, they are being familiarized with current digital technology and the skills to implement complex, sophisticated designs. However, working with FGPAs comes at a cost of increased complexity, notably the mastering of an HDL language, such as Verilog. Therefore, this book accomplishes the following: first, it teaches basic digital design concepts and then applies them through exercises; second, it implements these digital designs by teaching the user the syntax of the Verilog language while implementing the exercises. Finally, it employs contemporary digital hardware, such as the FPGA, to build a simple calculator, a basic music player, a frequency and period counter and it ends with a microprocessor being embedded in the fabric of the FGPA to communicate with the PC. In the process, readers learn about digital mathematics and digital-to-analog converter concepts through pulse width modulation.

Digital Logic Design Using Verilog Pearson Education

This book is an introduction into digital design with the focus on using the hardware construction language Chisel. Chisel brings advances from software engineering, such as object-orientated and functional languages, into digital design.This book addresses hardware designers and software engineers. Hardware designers, with knowledge of Verilog or VHDL, can upgrade their productivity with a modern language for their next ASIC or FPGA design. Software engineers, with knowledge of object-oriented and functional programming, can leverage their knowledge to program hardware, for example, FPGA accelerators executing in the cloud.The approach of this book is to present small to medium-sized typical hardware components to explore digital design with Chisel.

Make: FPGAs Springer Science & Business Media

by Phil Moorby The Verilog Hardware Description Language has had an amazing impact on the mod em electronics industry, considering that the essential composition of the language was developed in a surprisingly short period of time, early in 1984. Since its introduc tion, Verilog has changed very little. Over time, users have requested many improve ments to meet new methodology needs. But, it is a complex and time consuming process to add features to a language without ambiguity, and maintaining consistency. A group of Verilog enthusiasts, the IEEE 1364 Verilog committee, have broken the Verilog feature doldrums. These individuals should be applauded. They invested the time and energy, often their personal time, to understand and resolve an extensive wish-list of language enhancements. They took on the task of choosing a feature set that would stand up to the scrutiny of the standardization process. I would like to per sonally thank this group. They have shown that it is possible to evolve Verilog, rather than having to completely start over with some revolutionary new language. The Verilog 1364-2001 standard provides many of the advanced building blocks that users have requested. The enhancements include key components for verification, abstract design, and other new methodology capabilities. As designers tackle advanced issues such as automated verification, system partitioning, etc., the Verilog standard will rise to meet the continuing challenge of electronics design.

A Guide to Using SystemVerilog for Hardware Design and Modeling "O'Reilly Media, Inc."

As digital circuit elements decrease in physical size, resulting in increasingly complex systems, a basic logic model that can be used in the control and design of a range of semiconductor devices is vital. Finite State Machines (FSM) have numerous advantages; they can be applied to many areas (including motor control, and signal and serial data identification to name a few) and they use less logic than their alternatives, leading to the development of faster digital hardware systems. This clear and logical book presents a range of novel techniques for the rapid and reliable design of digital systems using FSMs, detailing exactly how and where they can be implemented. With a practical approach, it covers synchronous and asynchronous FSMs in the design of both simple and complex systems, and Petri-Net design techniques for sequential/parallel control systems. Chapters on Hardware Description Language cover the widely-used and powerful Verilog HDL in sufficient detail to facilitate the description and verification of FSMs, and FSM based systems, at both the gate and behavioural levels. Throughout, the text incorporates many real-world examples that demonstrate designs such as data acquisition, a memory tester, and passive serial data monitoring and detection, among others. A useful accompanying CD offers working Verilog software tools for the capture and simulation of design solutions. With a linear programmed learning format, this book works as a concise guide for the practising digital designer. This book will also be of importance to senior students and postgraduates of electronic engineering, who require design skills for the embedded systems market.

Optimized ASIP Synthesis from Architecture Description Language Models Springer Science & Business Media

Convergence and Hybrid Information Technology5th International Conference, ICHIT 2011, Daejeon, Korea, September 22-24, 2011, ProceedingsSpringer Science & Business Media

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