Applied Formal Verification For Digital Circuit Design 1st Edition

DYER DIAZ

19th International Conference, SAFECOMP 2000, Rotterdam, The Netherlands, October 24-27, 2000 Proceedings Springer Science & Business Media
This book constitutes the refereed proceedings of the 11th International Conference on Theorem Proving in Higher Order Logics, TPHOLs '98, held in Canberra, Australia, in September/October 1998. The 26 revised full papers presented were carefully reviewed and selected from a total of 52 submissions. Also included are two invited papers. The papers address all current aspects of theorem proving in higher order logics and formal verification and program analysis. Besides the HOL system, the theorem provers Coq, Isabelle, LAMBDA, LEGO, NuPrl, and PVS are discussed.
The Second NASA Formal Methods Workshop 1992 Springer Science & Business Media
This state-of-the-art monograph presents a coherent survey of a variety of methods and systems for formal hardware verification. It emphasizes the presentation of approaches that have matured into tools and systems usable for the actual verification of nontrivial circuits. All in all, the book is a representative and well-structured survey on the success and future potential of formal methods in proving the correctness of circuits. The various chapters describe the respective approaches supplying theoretical foundations as well as taking into account the application viewpoint. By applying all methods and systems presented to the same set of IFIP WG10.5 hardware verification examples, a valuable and fair analysis of the strenghts and weaknesses of the various approaches is given.
... Proceedings Morgan Kaufmann
CHARME'99 is the tenth in a series of working conferences devoted to the dev- opment and use of leading-edge formal techniques and tools for the design and veri?cation of hardware and systems. Previous conferences have been held in Darmstadt (1984), Edinburgh (1985), Grenoble (1986), Glasgow (1988), Leuven (1989), Torino (1991), Arles (1993), Frankfurt (1995) and Montreal (1997). This workshop and conference series has been organized in cooperation with IFIP WG 10. 5. It is now the biannual counterpart of FMCAD, which takes place every even-numbered year in the USA. The 1999 event took place in Bad Her- nalb, a resort village located in the Black Forest close to the city of Karlsruhe. The validation of functional and timing behavior is a major bottleneck in current VLSI design systems. A predominantly academic area of study until a few years ago, formal design and veri?cation techniques are now migrating into industrial use. The aim of CHARME'99 is to bring together researchers and users from academia and industry working in this active area of research. Two invited talks illustrate major current trends: the presentation by G´erard Berry (Ecole des Mines de Paris, Sophia-Antipolis, France) is concerned with the use of synchronous languages in circuit design, and the talk given by Peter Jansen (BMW, Munich, Germany) demonstrates an application of formal methods in an industrial environment. The program also includes 20 regular presentations and 12 short presentations/poster exhibitions that have been selected from the 48 submitted papers.
High-Level Verification Springer
A presentation of real examples of industrial uses for formalmethods such as SCADE, the B-Method, ControlBuild, Matelo, etc. invarious fields, such as railways, aeronautics, and the automotiveindustry, the purpose of this book is to present a summary ofexperience on the use of these "formal methods" (suchas proof and model-checking) in industrial examples of

complexsystems. It is based on the experience of people who are currently involvedin the creation and evaluation of safety critical system software.The involvement of people from within the industry allows us toavoid the usual problems of confidentiality which could arise andthus enables us to supply new useful information (photos,architecture plans, real examples, etc.).

Formal Hardware Verification Springer

Given the growing size and heterogeneity of Systems on Chip (SOC), the design process from initial specification to chip fabrication has become increasingly complex. This growing complexity provides incentive for designers to use high-level languages such as C, SystemC, and SystemVerilog for system-level design. While a major goal of these high-level languages is to enable verification at a higher level of abstraction, allowing early exploration of system-level designs, the focus so far for validation purposes has been on traditional testing techniques such as random testing and scenario-based testing. This book focuses on high-level verification, presenting a design methodology that relies upon advances in synthesis techniques as well as on incremental refinement of the design process. These refinements can be done manually or through elaboration tools. This book discusses verification of specific properties in designs written using high-level languages, as well as checking that the refined implementations are equivalent to their high-level specifications. The novelty of each of these techniques is that they use a combination of formal techniques to do scalable verification of system designs completely automatically. The verification techniques presented in this book include methods for verifying properties of high-level designs and methods for verifying that the translation from high-level design to a low-level Register Transfer Language (RTL) design preserves semantics. Used together, these techniques guarantee that properties verified in the high-level design are preserved through the translation to low-level RTL.

Formal Methods and Algorithms Springer

This book is a solid foundation of the most important formalisms used for specification and verification of reactive systems. In particular, the text presents all important results on m-calculus, w-automata, and temporal logics, shows the relationships between these formalisms and describes state-of-the-art verification procedures for them. It also discusses advantages and disadvantages of these formalisms, and shows up their strengths and weaknesses. Most results are given with detailed proofs, so that the presentation is almost self-contained. Includes all definitions without relying on other material Proves all theorems in detail Presents detailed algorithms in pseudo-code for verification as well as translations to other formalisms

Correct Hardware Design and Verification Methods CRC Press

Integrating formal property verification (FPV) into an existing design process raises several interesting questions. This book develops the answers to these questions and fits them into a roadmap for formal property verification – a roadmap that shows how to glue FPV technology into the traditional validation flow. The book explores the key issues in this powerful technology through simple examples that mostly require no background on formal methods.

Assertion-Based Design Springer Science & Business Media

This book provides readers with a comprehensive introduction to the formal verification of hardware and software. World-leading experts from the domain of formal proof techniques show the latest developments starting from electronic system level (ESL) descriptions down to the register transfer level (RTL). The authors demonstrate at different abstraction layers how formal methods can help to ensure functional correctness. Coverage includes the latest academic research results, as well as descriptions of industrial tools and case studies.

Handbook of Model Checking Springer

The first edition of Principles of Verifiable RTL Design offered a common sense method for simplifying and unifying assertion specification by creating a set of predefined specification modules that could be instantiated within the designer's RTL. Since the release of the first edition, an entire industry-wide initiative for assertion specification has emerged based on ideas presented in the first edition. This initiative, known as the Open Verification Library Initiative (www.verificationlib.org), provides an assertion interface standard that enables the design engineer to capture many interesting properties of the design and precludes the need to introduce new HDL constructs (i.e., extensions to Verilog are not required). Furthermore, this standard enables the design engineer to `specify once,' then target the same RTL assertion specification over multiple verification processes, such as traditional simulation, semi-formal and formal verification tools. The Open Verification Library Initiative is an empowering technology that will benefit design and verification engineers while providing unity to the EDA community (e.g., providers of testbench generation tools, traditional simulators, commercial assertion checking support tools, symbolic simulation, and semi-formal and formal verification tools). The second edition of Principles of Verifiable RTL Design expands the discussion of assertion specification by including a new chapter entitled `Coverage, Events and Assertions'. All assertions exampled are aligned with the Open Verification Library Initiative proposed standard. Furthermore, the second edition provides expanded discussions on the following topics: start-up verification; the place for 4-state simulation; race conditions; RTL-style-synthesizable RTL (unambiguous mapping to gates); more `bad stuff'. The goal of the second edition is to keep the topic current. Principles of Verifiable RTL Design, A Functional Coding Style Supporting Verification Processes, Second Edition tells you how you can write Verilog to describe chip designs at the RTL level in a manner that cooperates with verification processes. This cooperation can return an order of magnitude improvement in performance and capacity from tools such as simulation and equivalence checkers. It reduces the labor costs of coverage and formal model checking by facilitating communication between the design engineer and the verification engineer. It also orients the RTL style to provide more useful results from the overall verification process.

CRC Press

Formal verification is a powerful new digital design method In this cutting-edge tutorial, two of the field's best known authors team up to show designers how to efficiently apply Formal Verification, along with hardware description languages like Verilog and VHDL, to more efficiently solve real-world design problems.

A System Level Perspective Princeton University Press

In the decade since the idea of adapting the evidence-based paradigm for software engineering was first proposed, it has become a major tool of empirical software engineering. Evidence-Based Software Engineering and Systematic Reviews provides a clear introduction to the use of an evidence-based model for software engineering research and practice.

Formal Specification and Verification of Digital Systems Applied Formal VerificationFor Digital Circuit Design

Formal Verification: An Essential Toolkit for Modern VLSI Design presents practical approaches for design and validation, with hands-on advice to help working engineers integrate these techniques into their work. Formal Verification (FV) enables a designer to directly analyze and mathematically explore the quality or other aspects of a Register Transfer Level (RTL) design without using simulations. This can reduce time spent validating designs and more quickly reach a final design for manufacturing. Building on a basic knowledge of SystemVerilog, this book demystifies FV and presents the practical applications that are bringing it into mainstream design and validation processes at Intel and other companies. After reading this book, readers will be prepared to introduce FV in their organization and effectively deploy FV techniques to increase design and validation productivity. Learn formal verification algorithms to gain full coverage without exhaustive simulation Understand formal verification tools and how they differ from simulation tools Create instant test benches to gain insight into how models work and find initial bugs Learn from Intel insiders sharing their hard-won knowledge and solutions to complex design problems

Computer Safety, Reliability, and Security Springer Science & Business Media

Formal verification is a powerful new digital design method. In this cutting-edge tutorial, two of the field's best known authors team up to show designers how to efficiently apply Formal Verification, along with hardware description languages like Verilog and VHDL, to more efficiently solve real-world design problems. Contents: Simulation-Based Verification * Introduction to Formal Techniques * Contrasting Simulation vs. Formal Techniques * Developing a Formal Test Plan * Writing High-Level Requirements * Proving High-Level Requirements * System Level Simulation * Design Example * Formal Test Plan * Final System Simulation

26th International Conference, FMICS 2021, Paris, France, August 24–26, 2021, Proceedings Clarendon Press

Now available in a three-volume set, this updated and expanded edition of the bestselling Digital Signal Processing Handbook continues to provide the engineering community with authoritative coverage of the fundamental and specialized aspects of information-bearing signals in digital form. Encompassing essential background material, technical details, standards, and software, The Digital Signal Processing Handbook, Second Edition reflects cutting-edge information on signal processing algorithms and protocols related to speech, audio, multimedia, and video processing technology associated with standards ranging from WiMax to MP3 audio, low-power/high-performance DSPs, color image processing, and chips on video. The three-volume set draws on the experience of leading engineers, researchers, and scholars and includes 29 new chapters that address multimedia and Internet technologies, tomography, radar systems, architecture, standards, and future applications in speech, acoustics, video, radar, and telecommunications. Each volume in the set is also available individually ... Emphasizing theoretical concepts, Digital Signal Processing Fundamentals (Catalog no. 46063) provides comprehensive coverage of the basic foundations of DSP. Coverage includes: Signals and Systems, Signal Representation and Quantization, Fourier Transforms, Digital Filtering, Statistical Signal Processing, Adaptive Filtering, Inverse Problems and Signal Reconstruction, and Time–Frequency and Multirate Signal Processing. Wireless, Networking, Radar, Sensor Array Processing, and Nonlinear Signal Processing (Catalog no. 46047) thoroughly covers the foundations of signal processing related to wireless, radar, space–time coding, and mobile communications together with associated applications to networking, storage, and communications. Video, Speech, and Audio Signal Processing and Associated Standards, (Catalog no. 4608X) details the basic foundations of speech, audio, image, and video processing and associated applications to broadcast, storage, search and retrieval, and communications.

Formal Methods and Digital Systems Validation for Airborne Systems Springer Science & Business Media

Integrated circuit capacity follows Moore's law, and chips are commonly produced at the time of this writing with over 70 million gates per device. Ensuring correct functional behavior of such large designs before fabrication poses an extremely challenging problem. Formal verification validates the correctness of the implementation of a design with respect to its specification through mathematical proof techniques. Formal techniques have been emerging as commercialized EDA tools in the past decade. Simulation remains a predominantly used tool to validate a design in industry. After more than 50 years of development, simulation methods have reached a degree of maturity, however, new advances continue to be developed in the area. A simulation approach for functional verification can theoretically validate all possible behaviors of a design but requires excessive computational resources. Rapidly evolving markets demand short design cycles while the increasing complexity of a design causes simulation approaches to provide less and less coverage. Formal verification is an attractive alternative since 100% coverage can be achieved; however, large designs impose unrealistic computational requirements. Combining formal verification and simulation into a single integrated circuit validation framework is an attractive alternative. This book focuses on an Integrated Design Validation (IDV) system that provides a framework for design validation and takes advantage of current technology in the areas of simulation and formal verification resulting in a practical validation engine with reasonable runtime. After surveying the basic principles of formal verification and simulation, this book describes the IDV approach to integrated circuit functional validation. Table of Contents: Introduction / Formal Methods Background / Simulation Approaches / Integrated Design Validation System / Conclusion and Summary

Applied Formal Verification : For Digital Circuit Design World Scientific

This book constitutes the refereed proceedings of the Second International Conference on E-learning and Games, Edutainment 2007, held in Hong Kong, China, in June 2007. It covers virtual and augmented reality in game and education, virtual characters in games and education, e-learning platforms and tools, geometry in games and virtual reality, vision, imaging and video technology, as well as collaborative and distributed environments.

Specification and Verification of Systolic Arrays Springer Science & Business Media

This book is intended as an innovative overview of current formal verification methods, combined with an in-depth analysis of some advanced techniques to improve the scalability of these methods, and close the gap between design and verification in computer-aided design. Formal Verification: Scalable Hardware Verification with Symbolic Simulation explains current formal verification methods and provides an in-depth analysis of some advanced techniques to improve the scalability of these methods and close the gap between design and verification in computer-aided design. It provides the theoretical background required to present such methods and advanced techniques, i.e. Boolean function representations, models of sequential networks and, in particular, some novel algorithms to expose the disjoint support decompositions of Boolean functions, used in one of the scalable approaches.

Report from FM89: A Workshop on the Assessment of Formal Methods for Trustworthy Computer Systems 23–27 July 1989, Halifax, Canada Springer

Applied Formal VerificationFor Digital Circuit DesignMcGraw Hill Professional

Handbook of Logic in Artificial Intelligence and Logic Programming: Volume 5: Logic Programming Springer Science & Business Media
Model checking is a powerful approach for the formal verification of software. It automatically provides complete proofs of correctness, or explains, via counter-examples, why a system is not correct. Here, the author provides a well written and basic introduction to the new technique. The first part describes in simple terms the theoretical basis of model checking: transition systems as a formal model of systems, temporal logic as a formal language for behavioral properties, and model-checking algorithms. The second part explains how to write rich and structured temporal logic specifications in practice, while the third part surveys some of the major model checkers available.

Formal Methods in Computer-Aided Design Elsevier
This book grew out of a NATO Advanced Study Institute summer school that was held in Antalya, TUrkey from 26 May to 6 June 1997. The purpose of the summer school was to expose recent advances in the formal verification of systems composed of both logical and continuous time components. The course was structured in two parts. The first part covered theorem-proving, system automaton models, logics, tools, and complexity of verification. The second part covered modeling and verification of hybrid systems, i. e. , systems composed of a discrete event part and a continuous time part that interact with each other in novel ways. Along with advances in microelectronics, methods to design and build logical systems have grown progressively complex. One way to tackle the problem of ensuring the error-free operation of digital or hybrid systems is through the use of formal techniques. The exercise of comparing the formal specification of a logical system namely, what it is supposed to do to its formal operational description-what it actually does!-in an automated or semi-automated manner is called verification. Verification can be performed in an after-the-fact manner, meaning that after a system is already designed, its specification and operational description are regenerated or modified, if necessary, to match the verification tool at hand and the consistency check is carried out.

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