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Reduced-Pin and Enhanced ... - IEEE SA The four-pin Test Access Port (TAP) ensures the access to the test infrastructure using a common protocol to all test data operations irrespective of the device or its manufacturer. There are two pins dedicated to data shifting (TDI and TDO), one pin dedicated to control operations (TMS), and one to provide the test clock (TCK). Gatewaying IEEE 1149.1 and IEEE 1149.7 Test Access Ports The group continued as an IEEE working group to complete the final standard which then got the official name IEEE Std 1149.1, the IEEE Standard Test Access Port and Boundary-Scan Architecture. The standard was first released in 1990. Since then enhancements have been made and the latest update was done in 2013, see IEEE 1149.1-2013. JTAG

boundary-scan, firmly based on IEEE standards. The circuitry uses IEEE 1149.1-2001 as its foundation, providing complete backward compatibility, while aggressively adding features to support test and applications debug. It defines six classes of 1149.7 Test Access Ports (TAP.7s), T0-T5, with each class providing incremental capability, building on that of the lower level classes. IEEE-SA Grouper Template 5 JTAG Interface. The Joint Test Action Group (JTAG) port is an IEEE standard that defines a Test Access Port and Boundary Scan Architecture for digital integrated circuits and provides a standardized serial interface for controlling the associated test logic. The TAP, Instruction Register (IR), and Data Registers (DR) can be used to test the

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