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Computational Intelligence in Digital and Network Designs and Applications
A Textbook from Silicon Valley Polytechnic Institute
Design-for-Test Using Simulink and Stateflow
System-on-Chip Test Architectures

Testing of Digital Systems
An Introduction to Logic Circuit Testing
Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits
Digital Integrated Circuits
Theory and Applications
Logic Testing and Design for Testability
CTL for Test Information of Digital ICs
Design and Testing of Digital Microfluidic Biochips
Simulation in the Design of Digital Electronic Systems
Digital Logic Testing and Simulation
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Built-in-Self-Test and Digital Self-Calibration for RF SoCs Springer Science & Business Media
This updated printing of the leading text and reference in digital systems testing and testable design provides comprehensive, state-of-the-art coverage of the field. Included are extensive discussions of test generation, fault modeling for classic and new technologies, simulation, fault simulation, design for testability, built-in self-test, and diagnosis. Complete with numerous problems, this book is a must-have for test engineers, ASIC and system designers, and CAD developers, and advanced engineering students will find this book an invaluable tool to keep current with recent changes in the field.
Digital Circuit Testing and Testability MIT Press (MA)
Test and Design-for-Testability in Mixed-Signal Integrated Circuits deals with test and design for test of analog and mixed-signal integrated circuits. Especially in System-on-Chip (SoC), where different technologies are intertwined (analog, digital, sensors, RF); test is becoming a true bottleneck of present and future IC

projects. Linking design and test in these heterogeneous systems will have a tremendous impact in terms of test time, cost and proficiency. Although it is recognized as a key issue for developing complex ICs, there is still a lack of structured references presenting the major topics in this area. The aim of this book is to present basic concepts and new ideas in a manner understandable for both professionals and students. Since this is an active research field, a comprehensive state-of-the-art overview is very valuable, introducing the main problems as well as the ways of solution that seem promising, emphasizing their basis, strengths and weaknesses. In essence, several topics are presented in detail. First of all, techniques for the efficient use of DSP-based test and CAD test tools. Standardization is another topic considered in the book, with focus on the IEEE 1149.4. Also addressed in depth is the connecting design and test by means of using high-level (behavioural) description techniques, specific examples are given. Another issue is related to test techniques for well-defined classes of integrated blocks, like data converters and phase-locked-loops. Besides these specification-driven testing techniques, fault-driven approaches are described as they offer potential solutions which are more similar to digital test methods. Finally, in Design-for-Testability and Built-In-Self-Test, two other concepts that were taken from digital design, are introduced in an analog context and illustrated for the case of integrated filters. In summary, the purpose of this book is to provide a glimpse on recent research results in the area of testing mixed-signal integrated circuits, specifically in the topics mentioned above. Much of the work reported herein has been performed within cooperative European Research Projects, in which the authors of the different chapters have actively collaborated. It is a representative snapshot of the current state-of-the-art in this emergent field.

Electronic Design Automation for IC System Design, Verification, and Testing Springer Science & Business Media

Modern electronics testing has a legacy of more than 40 years. The introduction of new technologies, especially nanometer technologies with 90nm or smaller geometry, has allowed the semiconductor industry to keep pace with the increased performance-capacity demands from consumers. As a result, semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost. This book is a comprehensive guide to new VLSI Testing and Design-for-Testability techniques that will allow students, researchers, DFT practitioners, and VLSI designers to master quickly System-on-Chip Test architectures, for test debug and diagnosis of digital, memory, and analog/mixed-signal designs. Emphasizes VLSI Test principles and Design for Testability architectures, with numerous illustrations/examples. Most up-to-date coverage available, including Fault Tolerance, Low-Power Testing, Defect and Error Tolerance, Network-on-Chip (NOC) Testing, Software-Based Self-Testing, FPGA Testing, MEMS Testing, and System-In-Package (SIP) Testing, which are not yet available in any testing book. Covers the entire spectrum of VLSI testing and DFT architectures, from digital and analog, to memory circuits, and fault diagnosis and self-repair from digital to memory circuits. Discusses future nanotechnology test trends and challenges facing the nanometer design era; promising nanotechnology test techniques, including Quantum-Dots, Cellular Automata, Carbon-Nanotubes, and Hybrid

Semiconductor/Nanowire/Molecular Computing. Practical problems at the end of each chapter for students.

Digital Integrated Circuits Springer Science & Business Media

This book facilitates the VLSI-interested individuals with not only in-depth knowledge, but also the broad aspects of it by explaining its applications in different fields, including image processing and biomedical. The deep understanding of basic concepts gives you the power to develop a new application aspect, which is very well taken care of in this book by using simple language in explaining the concepts. In the VLSI world, the importance of hardware description languages cannot be ignored, as the designing of such dense and complex circuits is not possible without them. Both Verilog and VHDL languages are used here for designing. The current needs of high-performance integrated circuits (ICs) including low power devices and new emerging materials, which can play a very important role in achieving new functionalities, are the most interesting part of the book. The testing of VLSI circuits becomes more crucial than the designing of the circuits in this nanometer technology era. The role of fault simulation algorithms is very well explained, and its implementation using Verilog is the key aspect of this book. This book is well organized into 20 chapters. Chapter 1 emphasizes on uses of FPGA on various image processing and biomedical applications. Then, the descriptions enlighten the basic understanding of digital design from the perspective of HDL in Chapters 2–5. The performance enhancement with alternate material or geometry for silicon-based FET designs is focused in Chapters 6 and 7. Chapters 8 and 9 describe the study of bimolecular interactions with biosensing FETs. Chapters 10–13 deal with advanced FET structures available in various shapes, materials such as nanowire, HFET, and their comparison in terms of device performance metrics calculation. Chapters 14–18 describe different application-specific VLSI design techniques and challenges for analog and digital circuit designs. Chapter 19 explains the VLSI testability issues with the description of simulation and its categorization into logic and fault simulation for test pattern generation using Verilog HDL. Chapter 20 deals with a secured VLSI design with hardware obfuscation by hiding the IC’s structure and function, which makes it much more difficult to reverse engineer.

Design of High Speed Interconnects and Signaling Springer Science & Business Media

An Introduction to Logic Circuit Testing provides a detailed coverage of techniques for test generation and testable design of digital electronic circuits/systems. The material covered in the book should be sufficient for a course, or part of a course, in digital circuit testing for senior-level undergraduate and first-year graduate students in Electrical Engineering and Computer Science. The book will also be a valuable resource for engineers working in the industry. This book has four chapters. Chapter 1 deals with various types of faults that may occur in very large scale integration (VLSI)-based digital circuits. Chapter 2 introduces the major concepts of all test generation techniques such as redundancy, fault coverage, sensitization, and backtracking. Chapter 3 introduces the key concepts of testability, followed by some ad hoc design-for-testability rules that can be used to enhance testability of combinational circuits. Chapter 4 deals with test generation and response evaluation

techniques used in BIST (built-in self-test) schemes for VLSI chips. Table of Contents: Introduction / Fault Detection in Logic Circuits / Design for Testability / Built-in Self-Test / References

Using HDL Models and Architectures Academic Press

In the past few years, reliable hardware system design has become increasingly important in the computer industry. Digital Circuit Testing and Testability is an easy to use introduction to the practices and techniques in this field.Parag K. Lala writes in a user-friendly and tutorial style, making the book easy to read, even for the newcomer to fault-tolerant system design. Each informative chapter is self-contained, with little or no previous knowledge of a topic assumed. Extensive references follow each chapter, making further research in a particular area readily available. Each chapter covers a different aspect or technological component of fault-tolerant system design, and this book is an excellent compilation of up-to-date information in an area where such a book is needed.

Design-for-Test Using Simulink and Stateflow John Wiley & Sons

This book is a comprehensive guide to new DFT methods that will show the readers how to design a testable and quality product, drive down test cost, improve product quality and yield, and speed up time-to-market and time-to-volume. Most up-to-date coverage of design for testability. Coverage of industry practices commonly found in commercial DFT tools but not discussed in other books. Numerous, practical examples in each chapter illustrating basic VLSI test principles and DFT architectures.

Test and Design-for-Testability in Mixed-Signal Integrated Circuits Cambridge University Press

From the reviews: "[...] a welcome addition to the literature. [...] This book promises to make a valuable contribution to the education of graduate students in electrical and computer engineering, and a very useful addition to the library of the maturer investigator in SoC designs or related fields." Microelectronics Reliability

Design for Testability, Debug and Reliability Prentice Hall

"Introduces a theory of random testing in digital circuits for the first time and offers practical guidance for the implementation of random pattern generators, signature analyzers design for random testability, and testing results. Contains several new and unpublished results. "

Digital and Mixed Analogue/digital Techniques Digital System Test and Testable DesignUsing HDL Models and Architectures

The first book devoted to quantum-dot cellular automata (QCA), this groundbreaking resource provides a comprehensive view of QCA, showing practitioners how to work with this cutting-edge technology.

Design for Testability CRC Press

The modern electronic testing has a forty year history. Test professionals hold some fairly large conferences and numerous workshops, have a journal, and there are over one hundred books on testing. Still, a full course on testing is offered only at a few universities, mostly by professors who have a research interest in this area. Apparently, most professors would not have taken a course on electronic testing when they were students. Other than the computer engineering curriculum being too crowded, the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook. For VLSI the foundation was provided by semiconductor device techn- ogy, circuit design,

and electronic testing. In a computer engineering curriculum, therefore, it is necessary that foundations should be taught before applications. The field of VLSI has expanded to systems-on-a-chip, which include digital, memory, and mixed-signalsubsystems. To our knowledge this is the first textbook to cover all three types of electronic circuits. We have written this textbook for an undergraduate "foundations" course on electronic testing. Obviously, it is too voluminous for a one-semester course and a teacher will have to select from the topics. We did not restrict such freedom because the selection may depend upon the individual expertise and interests. Besides, there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course. With equal tenacity, we address the needs of three other groups of readers.

Advanced VLSI Design and Testability Issues Morgan & Claypool Publishers

Digital System Test and Testable DesignUsing HDL Models and ArchitecturesSpringer Science & Business Media

Design of Systems on a Chip: Design and Test Springer

This book provides a comprehensive methodology for automated design, test and diagnosis, and use of robust, low-cost, and manufacturable digital microfluidic systems. It focuses on the development of a comprehensive CAD optimization framework for digital microfluidic biochips that unifies different design problems. With the increase in system complexity and integration levels, biochip designers can utilize the design methods described in this book to evaluate different design alternatives, and carry out design-space exploration to obtain the best design point.

VLSI Test Principles and Architectures Morgan Kaufmann

This book discusses the digital design of integrated circuits under process variations, with a focus on design-time solutions. The authors describe a step-by-step methodology, going from logic gates to logic paths to the circuit level. Topics are presented in comprehensively, without overwhelming use of analytical formulations. Emphasis is placed on providing digital designers with understanding of the sources of process variations, their impact on circuit performance and tools for improving their designs to comply with product specifications. Various circuit-level "design hints" are highlighted, so that readers can use then to improve their designs. A special treatment is devoted to unique design issues and the impact of process variations on the performance of FinFET based circuits. This book enables readers to make optimal decisions at design time, toward more efficient circuits, with better yield and higher reliability.

Design for Test Methodology for Transition Fault Testing for Digital Design Elsevier

Device testing represents the single largest manufacturing expense in the semiconductor industry, costing over $40 billion a year. The most comprehensive and wide ranging book of its kind, Testing of Digital Systems covers everything you need to know about this vitally important subject. Starting right from the basics, the authors take the reader through automatic test pattern generation, design for testability and built-in self-test of digital circuits before moving on to more advanced topics such as IDDQ testing, functional testing, delay fault testing, memory testing, and fault diagnosis. The book includes detailed treatment of the latest techniques including test generation for various fault

models, discussion of testing techniques at different levels of integrated circuit hierarchy and a chapter on system-on-a-chip test synthesis. Written for students and engineers, it is both an excellent senior/graduate level textbook and a valuable reference.

EDA for IC System Design, Verification, and Testing Springer Nature

This book will introduce design methodologies, known as Built-in-Self-Test (BiST) and Built-in-Self-Calibration (BiSC), which enhance the robustness of radio frequency (RF) and millimeter wave (mmWave) integrated circuits (ICs). These circuits are used in current and emerging communication, computing, multimedia and biomedical products and microchips. The design methodologies presented will result in enhancing the yield (percentage of working chips in a high volume run) of RF and mmWave ICs which will enable successful manufacturing of such microchips in high volume.

Digital Circuit Testing Elsevier

Using the book and the software provided with it, the reader can build his/her own tester arrangement to investigate key aspects of analog-, digital- and mixed system circuits Plan of attack based on traditional testing, circuit design and circuit manufacture allows the reader to appreciate a testing regime from the point of view of all the participating interests Worked examples based on theoretical bookwork, practical experimentation and simulation exercises teach the reader how to test circuits thoroughly and effectively

Design-for-test for Digital IC's and Embedded Core Systems Springer Science & Business Media

Today's computers must perform with increasing reliability, which in turn depends onthe problem of determining whether a circuit has been manufactured properly or behaves correctly.However, the greater circuit density of VLSI circuits and systems has made testing more difficultand costly. This book notes that one solution is to develop faster and more efficient algorithms togenerate test patterns or use design techniques to enhance testability - that is, "design fortestability." Design for testability techniques offer one approach toward alleviating this situationby adding enough extra circuitry to a circuit or chip to reduce the complexity of testing. Becausethe cost of hardware is decreasing as the cost of testing rises, there is now a growing interest inthese techniques for VLSI circuits.The first half of the book focuses on the problem of testing:test generation, fault simulation, and complexity of testing. The second half takes up the problemof design for testability: design techniques to minimize test application and/or test generationcost, scan design for sequential logic circuits, compact testing, built-in testing, and variousdesign techniques for testable systems.Hideo Fujiwara is an associate professor in the Department ofElectronics and Communication, Meiji University. Logic Testing and Design for Testability isincluded in the Computer Systems Series, edited by Herb Schwetman.

Design for Testability, Fault Simulation and Test Generation in Digital Electronics CRC Press

Recent technological advances have created a testing crisis in the electronics industry--smaller, more highly integrated electronic circuits and new packaging techniques make it increasingly difficult to physically access test nodes. New testing methods are needed for the next generation of electronic

equipment and a great deal of emphasis is being placed on the development of these methods. Some of the techniques now becoming popular include design for testability (DFT), built-in self-test (BIST), and automatic test vector generation (ATVG). This book will provide a practical introduction to these and other testing techniques. For each technique introduced, the author provides real-world examples so the reader can achieve a working knowledge of how to choose and apply these increasingly important testing methods.
Computational Intelligence in Digital and Network Designs and Applications Artech House Publishers
A current trend in digital design-the integration of the MATLAB® components Simulink® and Stateflow® for model building, simulations, system testing, and fault detection-allows for better control over the design flow process and, ultimately, for better system results. Digital Integrated Circuits: Design-for-Test Using Simulink® and Stateflow® illustrates the construction of Simulink models for digital project test benches in certain design-for-test fields. The first two chapters of the book describe the major tools used for design-for-test. The author explains the process of Simulink model building, presents the main library blocks of Simulink, and examines the development of finite-state machine modeling using Stateflow diagrams. Subsequent chapters provide examples of Simulink modeling and simulation for the latest design-for-test fields, including combinational and sequential circuits, controllability, and observability; deterministic algorithms; digital circuit dynamics; timing verification; built-in self-test (BIST) architecture; scan cell operations; and functional and diagnostic testing. The book also discusses the automatic test pattern generation (ATPG) process, the logical determinant theory, and joint test action group (JTAG) interface models. Digital Integrated Circuits explores the possibilities of MATLAB's tools in the development of application-specific integrated circuit (ASIC) design systems. The book shows how to incorporate Simulink and Stateflow into the process of modern digital design.

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