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Rules. In PCB design, to achieve the optimum routing path, it requires both proper DIMM connector placement and proper memory chip use. In general, DDR4 SDRAM requires shorter routes and the appropriate spacing for peak timing and optimal signal integrity. PCB designers should also employ pin swapping in the relevant signal groups. **DDR4 Routing Guidelines for PCB and the Advancements in ...** As Cavium has enhanced its PCB design process, Munroe notes that when routing DDR4 designs, it's best to route signals spaced at 5X the line width for better noise/coupling immunity. "I get a true serpentine and all of the lengths I'm looking for. My rule of thumb: if the space is available, use it," he said. **4X Faster Timing Closure on High-Speed Interfaces with ...** <sup>23</sup> When routing the data lanes, route the outer-most (that is, the longest lane) first, because this determines the amount of trace length to add on the inner data lanes. <sup>24</sup> Route all signals within a given byte lane on the same critical layer with the same via count. Assuming ECC is used, the DDR4 data bus consists of nine data byte lanes. **AN5097, Hardware and Layout Design Considerations for DDR4 ...** **PCB Routing guidelines for Ultrascale DDR4 DIMM using x4 components** How should one route DQ/DQS when interfacing to x4 based dimms, that will never be x8 based dimms ? Should we have separate routing constraints for each nibble group, and allow clearance between nibble groups by routing on separate layers, with each nibble group having its own DQS to DQ rules and timing. **PCB Routing guidelines for Ultrascale DDR4 DIMM us ...** The Mini PC board contains two onboard 8 GB DDR4 DRAM chips running at 1866 MHz, and routing between the FPGA and DDR4 chips

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