Cmos Test And Evaluation A Physical Perspective

Testing of Digital CMOS Integrated Circuits
Testing and Design of CMOS D-Latches
Testing of Digital Systems
Evaluation of Dynamic Current Testing for CMOS Domino Circuits
Test Generation and Evaluation for Bridging Faults in CMOS VLSI Circuits
Defect Classes - an Overdue Paradigm for CMOS IC Testing
Testing a CMOS Operational Amplifier Circuit Using a Combination of Oscillation and IDDQ Test Methods
A Process Development and Quality Evaluation Test Chip for Double-level Metal CMOS
The Design, Testing, and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control
Electrical Testing of a CMOS Baseline Process
Journal of Testing and Evaluation
CMOS Life Suitability Evaluation Program

CMOS/SOS Test Patterns for Process Evaluation and Control
CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies
Dynamic Power Supply Current Testing
Testing and Design for Testability of CMOS Logic Circuits
Iddq Testing for CMOS VLSI
Introduction to IDDQ Testing
CMOS/SOS Test Patterns for Process Evaluation and Control
Wafer Level Reliability of Advanced CMOS Devices and Processes
Automatic Testing and Evaluation of Digital Integrated Circuits
Design, Testing and Analysis of Test Patterns for CMOS Process Control and Monitoring
Testing and Reliable Design of CMOS Circuits
CMOS Test and Evaluation
CMOS circuit design and test patterns for built in overcurrent testing
Evaluation of a CMOS/SOS Process Using Process Validation Wafers
Comparing Stuck Fault and Current Testing Via CMOS Chip Test
ESD Testing
Gamma Irradiation Testing of Electronic Devices, and Evaluation of Irradiated CMOS Components on MOSIS Test Chips
Rapid Reliability Assessment of VLSICs

CMOS Electronics
Design and Experimental Evaluation of a 3rd Generation Addressable CMOS Piezoresistive Stress Sensing Test Chip
Quiescent Current Testing of CMOS Data Converters
IDDQ Testing of VLSI Circuits
Stuck Fault and Current Testing Comparison Using CMOS Chip Test
Microelectronic Test Structures for CMOS Technology
Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits
Principles of Testing Electronic Systems
Design, Testing, and Analysis of a Co-Prehensivs Test Pattern for Measuring CMOS/SOS Process Performance and Control
CMOS VLSI

Cmos Test And Evaluation A Physical Perspective

Downloaded from archive.imba.com ***by guest***

KODY LEBLANC

Testing of Digital CMOS Integrated Circuits Cambridge University Press Microelectronic Test Structures for CMOS Technology and Products addresses the basic concepts of the design of test structures for incorporation within test-vehicles, scribe-lines, and CMOS products. The role of test structures in the development and monitoring of CMOS technologies and products has

become ever more important with the increased cost and complexity of development and manufacturing. In this timely volume, IBM scientists Manjul Bhushan and Mark Ketchen emphasize high speed characterization techniques for digital CMOS circuit applications and bridging between circuit performance and characteristics of MOSFETs and other circuit elements. Detailed examples are presented throughout, many of which are equally applicable to other microelectronic technologies as well. The authors' overarching goal is to provide students and technology practitioners alike a practical guide to the disciplined design and use of test structures that give unambiguous information on the parametrics and performance of digital CMOS technology.

Testing and Design of CMOS D-Latches
Springer Science & Business Media
The definition from SEMATECH of wafer level reliability test is: a methodology to assess the reliability impact of tools and processes by testing mechanism-specific test structures under accelerated conditions during device processing. Because wafer level reliability test is the accelerated test, it owns some different characters with common long time test in terms of failure mechanisms, test procedures, life time prediction, test structures design and so on. In this book, all items of wafer level reliability of CMOS devices and processes will be discussed. The purpose of this book is to provide a good and urgently need reference on MOS device reliability. The authors discuss how to enhance the

veracity of lifetime prediction and the effects to degrade the veracity deeply. Finally, a discussion of the problems with wafer level reliability in terms of the engineering applications and research is given.

Testing of Digital Systems CRC Press
The CMOS D-latch is an important block in the design of sequential circuits. Thus, a new fully testable CMOS D-latch (FTD) is proposed. A comprehensive test set that includes possible physical failures is developed. This test set is then applied to the FTD. The cost of implementation, analysis, and simulation of the FTD are all presented. Application of the FTD-latch to build a polarity-hold shift register is shown.

Evaluation of Dynamic Current Testing for CMOS Domino Circuits
Springer Science & Business Media
CMOS Test and Evaluation: A Physical Perspective is a single source for an integrated view of test and data analysis methodology for CMOS products, covering circuit sensitivities to MOSFET characteristics, impact of silicon technology process variability, applications of embedded test structures and sensors, product yield, and reliability over the lifetime of the product. This book also covers statistical data analysis and visualization techniques, test equipment and CMOS product specifications, and examines product behavior over its full voltage, temperature and frequency range.

Test Generation and Evaluation for Bridging Faults in CMOS VLSI Circuits
John Wiley & Sons

An efficient automatic test pattern generator for I$sb{DDQ}$ current testing of CMOS digital circuits is presented. The complete two-line bridging fault set is considered. Because of the time constraints of I$sb{DDQ}$ testing, an adaptive genetic algorithm (GA) is used to generate compact test sets. To accurately evaluate the test sets, fault grading is performed using a switch-level fault simulator and a mixed-mode electrical-level fault simulator. The test sets are compared with those generated by HITEC, a traditional gate-level test generator. Experimental results for ISCAS85 and ISCAS89 benchmark circuits are presented. The results show that for I$sb{DDQ}$ testing, the GA test sets outperform the HITEC test sets. When the test sets are truncated due to test time constraints, the fault coverages can differ by 10% or more. In addition to test generation and test evaluation, diagnosis (fault location) is also performed using both test sets. Diagnosis is performed using fault dictionaries constructed during test evaluation. In addition to the traditional full dictionary, two reduced dictionaries are also presented. The results show that the reduced dictionaries offer good size-resolution trade-offs when compared with the full dictionary.
Defect Classes - an Overdue Paradigm for CMOS IC Testing Artech House Publishers
A pragmatic approach to testing electronic systems As we move ahead in the electronic age, rapid changes in technology pose an ever-increasing

number of challenges in testing electronic products. Many practicing engineers are involved in this arena, but few have a chance to study the field in a systematic way-learning takes place on the job. By covering the fundamental disciplines in detail, Principles of Testing Electronic Systems provides design engineers with the much-needed knowledge base. Divided into five major parts, this highly useful reference relates design and tests to the development of reliable electronic products; shows the main vehicles for design verification; examines designs that facilitate testing; and investigates how testing is applied to random logic, memories, FPGAs, and microprocessors. Finally, the last part offers coverage of advanced test solutions for today's very deep submicron designs. The authors take a phenomenological approach to the subject matter while providing readers with plenty of opportunities to explore the foundation in detail. Special features include: * An explanation of where a test belongs in the design flow * Detailed discussion of scan-path and ordering of scan-chains * BIST solutions for embedded logic and memory blocks * Test methodologies for FPGAs * A chapter on testing system on a chip * Numerous references

Testing a CMOS Operational Amplifier Circuit Using a Combination of Oscillation and IDDQ Test Methods

Springer Science & Business Media

Advances in design methods and process technologies have resulted in a continuous increase in the complexity of

integrated circuits (ICs). However, the increased complexity and nanometer-size features of modern ICs make them susceptible to manufacturing defects, as well as performance and quality issues. Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens/bridges, and design-for-manufacturing (DfM)-related rule violations. The book also addresses testing for small-delay defects (SDDs), which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing, including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on "alternative methods" that explores new metrics, top-off ATPG, and circuit topology-based solutions Highlights the advantages and disadvantages of a diverse set of metrics, and identifies scope for improvement Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions.

A Process Development and Quality

Evaluation Test Chip for Double-level Metal CMOS Springer Science & Business Media

The objective of this work was to determine baseline electrical parameters that could be used to evaluate a fabrication process. Two lots of wafers containing NBS-16 test chips were fabricated at a commercial vendor in a radiation-hard, CMOS/SOS process. These wafers were then returned to NBS for testing and evaluation. Testing was performed using an automated computer-controlled integrated circuit test system. Test results were evaluated using analysis techniques which provided a statistical estimate of selected parameters and identified spatial correlations between data sets. Further analysis was then performed in order to identify process irregularities. A complete description of the test results and analysis procedure can be found in the appendices.

The Design, Testing, and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control John Wiley & Sons

The increasing application of integrated circuits in situations where high reliability is needed places a requirement on the manufacturer to use methods of testing to eliminate devices that may fail on service. One possible approach that is described in this book is to make precise electrical measurements that may reveal those devices more likely to fail. The measurements assessed are of analog

circuit parameters which, based on a knowledge of failure mechanisms, may indicate a future failure. . To incorporate these tests into the functional listing of very large scale integrated circuits consideration has to be given to the sensitivity of the tests where small numbers of devices may be defective in a complex circuit. In addition the tests ideally should require minimal extra test time. A range of tests has been evaluated and compared with simulation used to assess the sensitivity of the measurements. Other work in the field is fully referenced at the end of each chapter. The team at Lancaster responsible for this book wish to thank the Alvey directorate and SERe for the necessary support and encouragement to publish our results. We would also like to thank John Henderson, recently retired from the British Telecom Research Laboratories, for his cheerful and enthusiastic encouragement. Trevor Ingham, now in New Zealand, is thanked for his early work on the project.

Electrical Testing of a CMOS Baseline Process Springer

Testing techniques for VLSI circuits are undergoing many exciting changes. The predominant method for testing digital circuits consists of applying a set of input stimuli to the IC and monitoring the logic levels at primary outputs. If, for one or more inputs, there is a discrepancy between the observed output and the expected output then the IC is declared to be defective. A new approach to testing digital circuits, which has come to be known as IDDQ testing,

has been actively researched for the last fifteen years. In IDDQ testing, the steady state supply current, rather than the logic levels at the primary outputs, is monitored. Years of research suggests that IDDQ testing can significantly improve the quality and reliability of fabricated circuits. This has prompted many semiconductor manufacturers to adopt this testing technique, among them Philips Semiconductors, Ford Microelectronics, Intel, Texas Instruments, LSI Logic, Hewlett-Packard, SUN microsystems, Alcatel, and SGS Thomson. This increase in the use of IDDQ testing should be of interest to three groups of individuals associated with the IC business: Product Managers and Test Engineers, CAD Tool Vendors and Circuit Designers. Introduction to IDDQ Testing is designed to educate this community. The authors have summarized in one volume the main findings of more than fifteen years of research in this area.

Journal of Testing and Evaluation

Springer

This book discusses in detail the correlation between physical defects and logic faults, and shows you how Iddq testing locates these defects. The book provides planning guidelines and optimization methods and is illustrated with numerous examples ranging from simple circuits to extensive case studies.

CMOS Life Suitability Evaluation Program

Springer Science & Business Media

The results of a matrix of high-temperature accelerated life tests, 125C life tests, and 250 hour 250C lot

acceptance tests were evaluated to determine the reliabiltiy of a cross-section of the complementary metal oxide semiconductor (CMOS) family of devices. The devices evaluated included a NOR gate, a flip-flop, a four bit adder, and a counter/divider. Each device was procured from two different manufacturers, and from three different lots of each manufacturer. The correlation of the Lot Acceptance data with the reliability of the devices revealed that the Class S Lot Acceptance Test, as specified in MIL-STD-883, Method 500.5 is approximately 50% effective screening for lot reliability. To minimize the possibility of rejecting good lots and/or accepting bad lots, two temperature Lot Acceptance Test is recommended. Using a two temperature Lot Acceptance Test at temperature above 200 C would permit control of both the activation energy and pre-exponential factor in the Arrhenius model. A 100% burn-9n is also recommended. Although burn-in would not improve all lots, it would improve the reliability of those lots which have a freak population with a high failure rate.

CMOS/SOS Test Patterns for Process Evaluation and Control John Wiley & Sons

The IC test industry has struggled for more than 30 years to establish a test approach that would guarantee a low defect level to the customer. We propose a comprehensive strategy for testing CMOS ICs that uses defect classes based on measured defect electrical properties. Defect classes differ from traditional

fault models. Our defect class approach requires that the test strategy match the defect electrical properties, while fault models require that IC defects match the fault definition. We use data from Sandia Labs failure analysis and test facilities and from public literature. We describe test pattern requirements for each defect class and propose a test paradigm.

CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies

With the evolution of semiconductor technology and global diversification of the semiconductor business, testing of semiconductor devices to systems for electrostatic discharge (ESD) and electrical overstress (EOS) has increased in importance. ESD Testing: From Components to Systems updates the reader in the new tests, test models, and techniques in the characterization of semiconductor components for ESD, EOS, and latchup. Key features: Provides understanding and knowledge of ESD models and specifications including human body model (HBM), machine model (MM), charged device model (CDM), charged board model (CBM), cable discharge events (CDE), human metal model (HMM), IEC 61000-4-2 and IEC 61000-4-5. Discusses new testing methodologies such as transmission line pulse (TLP), to very fast transmission line pulse (VF-TLP), and future methods of long pulse TLP, to ultra-fast TLP (UF-TLP). Describes both conventional testing and new testing techniques for both chip and system level evaluation. Addresses EOS

testing, electromagnetic compatibility (EMC) scanning, to current reconstruction methods. Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing. ESD Testing: From Components to Systems is part of the authors' series of books on electrostatic discharge (ESD) protection; this book will be an invaluable reference for the professional semiconductor chip and system-level ESD and EOS test engineer. Semiconductor device and process development, circuit designers, quality, reliability and failure analysis engineers will also find it an essential reference. In addition, its academic treatment will appeal to both senior and graduate students with interests in semiconductor process, device physics, semiconductor testing and experimental work.

Dynamic Power Supply Current Testing

Abstract: "This paper compares the effectiveness of Stuck Fault and Current Testing, as applied to CMOS ICs. The comparison is performed by testing actual IC chips using patterns developed via both methods, and then contrasting their ability to identify faulty product. The test results indicate that, for the investigated set of chips, Current Testing can provide a dramatically better screen of defective product than by using Stuck Fault Testing itself."

Testing and Design for Testability of CMOS Logic Circuits

The monograph will be dedicated to SRAM (memory) design and test issues

in nano-scaled technologies by adapting the cell design and chip design considerations to the growing process variations with associated test issues. Purpose: provide process-aware solutions for SRAM design and test challenges.

Iddq Testing for CMOS VLSI

Piezoresistive stress sensing chips have been used extensively for measurement of assembly related die surface stresses. Although many experiments can be performed with resistive structures which are directly bonded, for extensive stress mapping it is necessary to have a large number of sensor cells which can be addressed using CMOS logic circuitry. Our previous test chip, the ATC04, has 100 cells, each approximately 0.012 in. on a side, on a chip with a side dimension of 0.45 in. When a cell resistor is addressed, it is connected to a four terminal measurement bus through CMOS transmission gates. In theory, the gate resistances do not affect the measurement. In practice, there may be subtle effects which appear when very high accuracy is required. At high temperatures, gate leakage can increase to a point at which the resistor measurement becomes inaccurate. For ATC04 this occurred at or above 50 C. Here, we report on the first measurements obtained with a new prototype test chip, the ATC06. This prototype was fabricated in a 0.5 micron feature size silicided CMOS process using the MOSIS prototyping facility. The cell size was approximately 0.004 in. on a side. In order to achieve piezoresistive

behavior for the implanted resistors it was necessary to employ a non-standard silicide ''blocking'' process. The stress sensitivity of both implanted and polysilicon blocked resistors is discussed. Using a new design strategy for the CMOS logic, it was possible to achieve a design in which only 5 signals had to be routed to a cell for addressing vs. 9 for ATC04. With our new design, the resistor under test is more effectively electrically isolated from other resistors on the chip, thereby improving high temperature performance. We present data showing operation up to 140 C.

Introduction to IDDQ Testing

Abstract: "This paper compares the effectiveness of Stuck Fault and Current Testing, as applied to CMOS ICs. The comparison is performed by testing sequential CMOS chips using patterns developed via both methods, and evaluating their ability to identify faulty product. The test results are then contrasted to a previous study in which a smaller, combinatorial chip was tested by the same means. The results indicate that, for the investigated set of chips, Current Testing provides a better screen of defective product for some classes of defects, while Stuck Fault Testing is more effective on others."

CMOS/SOS Test Patterns for Process Evaluation and Control

Transient current (iDDT) refers to the current drawn from the power supply durin g the transient switching of CMOS gates. Testing based on the transient current can detect many of the defects that can occur in ICs, such as resistive

opens, w hich may not be detected by traditional voltage testing or by Leakage current (I DDQ) testing methods. A major set back for IDDQ testing methods is the increased leakage currents in today's ICs. Thus iDDT based testing has been often investi gated as an alternative or supplement to (IDDQ) testing. Little work has focused on iDDT testing for domino circuits. In this thesis, we propose a method for testing domino CMOS circuits using the transient power supp ly current. The method is based on monitoring the peak value of the transient cu rrent. This peak varies considerably with process variations, so each process ha s different thresholds; this problem will be addressed by proposing a normalizat ion procedure that allows us to use a single threshold for all processes. We pre sent also a test vector generation algorithm for testing large domino circuits. We evaluate the effectiveness of this testing method by simulation on various do mino circuits of different sizes. We develop and implement a partitioning technique to improve the fault coverage of the test method when used with large circuits. The algorithm divides the circ uit into different clusters where each cluster is fed by a different power suppl y branch. We also provide an automation system to simplify the process of genera ting the simulation files, injecting the defects in the circuit, running the sim ulations, storing the simulations output, processing the output signals, and fin ally gathering and analyzing the results.

Wafer Level Reliability of Advanced

CMOS Devices and Processes

In the last few years CMOS technology has become increas ingly dominant for realizing Very Large Scale Integrated (VLSI) circuits. The popularity of this technology is due to its high den sity and low power requirement. The ability to realize very com plex circuits on a single chip has brought about a revolution in the world of electronics and computers. However, the rapid advance ments in this area pose many new problems in the area of testing. Testing has become a very time-consuming process. In order to ease the burden of testing, many schemes for designing the circuit for improved testability have been presented. These design for testability techniques have begun to catch the attention of chip manufacturers. The trend is towards placing increased emphasis on these techniques. Another byproduct of the increase in the complexity of chips is their higher susceptibility to faults. In order to take care of this problem, we need to build fault-tolerant systems. The area of fault-tolerant computing has steadily gained in importance. Today many universities offer courses in the areas of digital system testing and fault-tolerant computing. Due to the impor tance of CMOS technology, a significant portion of these courses may be devoted to CMOS testing. This book has been written as a reference text for such courses offered at the senior or graduate level. Familiarity with logic design and switching theory is assumed. The book should also prove to be useful to

professionals working in the semiconductor industry.

Related with Cmos Test And Evaluation A Physical Perspective:

- Poe Atlas Tree Guide : click here